CMOS-Compatible Long-Range Dielectric-Loaded Plasmonic Waveguides

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***Abstract*—CMOS-compatible long-range dielectric-loaded plasmonic waveguides featuring long propagation lengths and strong mode confinements are designed and studied using the finite-element method. The waveguide composition includes a Si_3N_4 ridge on the top of a thin metal stripe deposited on a silicon-on-insulator (SOI) wafer with a thin top SiO_2 layer produced by thermal oxidation. All the materials chosen in the design are compatible with complementary metal–oxide–semiconductor technology and can be integrated with plasmonic, electronic and photonic components. Influence of various waveguide parameters on the waveguide characteristics is analyzed, including the thicknesses of the Si layer and the SiO_2 layers, the dimension of the ridge, as well as the parameters of the metal stripe. It is found that, at the telecom wavelength of 1.55 μm, the propagation length of CMOS-plasmonic waveguides can reach 1.07 mm with a lateral mode confinement of $\sim$1.18 μm and 4.43 mm with a lateral mode width of $\sim$2.32 μm. The bending loss and coupling length are both calculated to evaluate the applicability of the proposed device for high density integration and a figure of merit is proposed to show the tradeoff between the propagation length and the lateral mode width in the application of plasmonic devices.**

***Index Terms*—CMOS-compatible plasmonic waveguides, Dielectric-loaded waveguides, long range surface plasmon, plasmonic waveguides.**

I. Introduction

ON-CHIP optical interconnection has been considered as a prospective technology to replace the conventional electrical interconnection because of its low power consumption, and its high transmission bandwidth [1]–[3].The development of conventional photonic circuits is hindered by diffraction limit, preventing their miniaturization toward the nanoscale which is required for integration with electronics. Plasmonic devices, operating at the subwavelength scale are considered as a viable solution, thus motivated the substantial research in the field of plasmonic waveguides based on surface plasmon polartions (SPPs) [4]. SPPs are surface electromagnetic waves propagating along a dielectric–metal interface near the speed of light. Their large momentum allows for strong mode confinement at subwavelength scale and enables the development of ultracompact-integrated photonic circuits [5].

Numerous plasmonic waveguides are reported in recent years including V-groove waveguides [6]–[8], gap waveguides [9]–[11], metallic nanowires [12]–[14], nanowires in microstructured fibers [15], nanofiber loaded waveguides [16], and so on. Dielectric-loaded SPP waveguides (DLSPPWs) which are formed with a dielectric ridge deposited on the surface of a metal film have got great attention and been demonstrated to be a suitable configuration to guide plasmonic modes at telecom wavelengths due to the tight mode confinement and low propagation loss [17]–[19]. Long-range DLSPPWs (LR-DLSPPWs) with a metal stripe embedded in dielectric layers are presented and demonstrated recently [20]–[22]. Long range SPPs can be considered as a coupled mode involving two SPP modes existing on the opposite sides of the thin metal film and the propagation length can research to several millimeters due to the mode coupling. The DLSPPWs and LR-DLSPPWs cannot only provide the transmission of light but also allows the transmission of electrical signal through the metal stripe, which can be used to control the light by electro-optic effect or thermo-optic effect, and makes it possible to incorporate active plasmonic elements, such as thermo-optic modulator, electro-optic modulator, optical switch, and so on [23], [24]. For these waveguides, the dimensions of the ridges are around 1000 nm $\times$ 1000 nm, which are large and comparable to that of a standard photonic waveguide. So the mode confinement of the propagation mode is mainly determined by the ridge and the thicknesses of the dielectric layers. The metal stripe can confine both the light and the electrical signal around the metal/dielectric interface and obtain very efficient thermo-optic or electro-optic effects.

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits, which is rapidly developing, following Moore's law. However, current bottleneck which slows down further progress is related to the problem of interconnection, which is now limited by the increasing resistance and the power consumption of the electric line in correspondence with the increase in signal frequency [25], [26]. Several CMOS-compatible SPP waveguides with subwavelength mode confinement have been proposed and demonstrated [27]–[30]. LR-DLSPPWs can be introduced into CMOS

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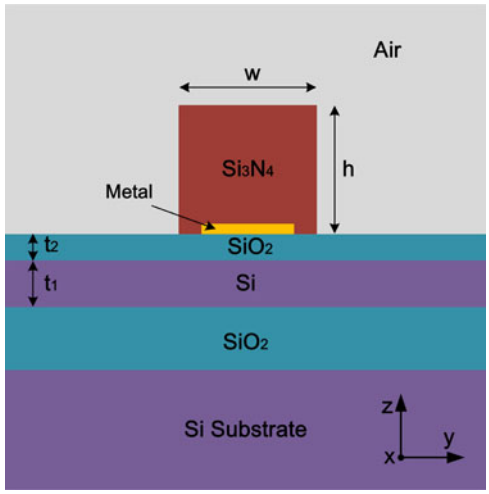

Fig. 1. Layout of the CMOS-compatible LR-DLSPPW structure, which consists of a thin metal film embedded between a dielectric ridge made of silicon nitride (Si_3N_4) and two dielectric layers (Si and SiO_2) which are supported by a $\sim$2–3 μm SiO_2 layer on top of a silicon substrate.

technology not only due to their strong mode confinement but also owing to the fact that these waveguides support relatively long propagation length, in the millimeter range, much longer than most of the SPP waveguides. To be compatible with CMOS technology, the materials of choice should be chosen such that they are supported by commercial semiconductor process. As an example, instead of using polymers one may choose silicon nitride, silicon dioxide, and silicon as the dielectric media. Aluminum or copper can be used as the metal stripe instead of gold or silver.

In this paper, we design and numerically investigate a CMOS-compatible long range dielectric-loaded SPP waveguide using finite-element method (FEM) simulations. The performance of such a CMOS-compatible LR-DLSPPW for different parameters is studied and optimized, and its advantages are demonstrated and discussed.

II. Waveguide Structure and Principle

The proposed structure of CMOS-compatible LR-DLSPPW is shown in Fig. 1. The waveguide consists of a thin metal film embedded between a dielectric ridge made of silicon nitride (Si_3N_4) and two dielectric layers (Si and SiO_2) which are supported by a $\sim$2–3-μm SiO_2 layer on top of a silicon substrate. Such a structure can be constructed using silicon on insulator (SOI) substrate, covered by a metallic film. The upper silicon nitride layer can be grown using plasma enhanced chemical vapor deposition (PECVD) at low temperatures, up to 300° C.

The configuration is studied using 2-D FEM simulations (COMSOL Multiphysics) at the wavelength of 1.55 μm with TM-polarization, which can be used to excite SPP mode. The combination of silicon (Si), having a refractive index of $n_s = 3.48$ [31], sandwiched between two layers of silicon dioxide (SiO_2), $n_0 = 1.45$ [31] is chosen as the material of the lower dielectric layer. 500 nm wide, 15 nm thick copper replaces gold as the metal stripe and the refractive index at the wavelength of 1.55 μm is $n_{Cu} = 0.606 + i8.92$ [31]. Silicon nitride (Si_3N_4) is chosen as the material of upper dielectric ridge because of its high refractive index ($n_r = 1.98$) [31] and CMOS-compatible characteristics.

Starting with an SOI wafer, the upper SiO_2 layer is formed by oxidizing the Si layer using thermal oxidation. The thickness of the Si layer decreases with the increase of the thickness of the SiO_2 layer at a ratio of 1 (silicon) to 2.27 (SiO_2) [32]. The initial thickness of Si layer is chosen to be t_0 and its final thickness is t_1. Thus, the thickness of upper SiO_2 layer is $t_2 = (t_0 - t_1) \times 2.27$.

The performance of the waveguide is evaluated by calculating the mode confinement and the propagation length. The mode confinement can be represented by mode area and lateral mode width. For compact photonic integration, the lateral crosstalk between adjacent waveguides determines how closely two waveguides can be placed and the bend loss experienced the power loss when the mode propagating around a bend waveguide. Minimization of the lateral crosstalk and the bending loss are required to accommodate as many plasmonic devices as possible on a chip, and the mode confinement can be represented by the lateral mode width which can be found by taking the width of the norm of the electric field at $1/e$ of its maximum value. Meanwhile, the propagation length can be obtained by taking the propagation length of the norm of the electric field at $1/e$ of its maximum value [21].

III. Simulation and Analysis

A. Influence of the Thicknesses of the Si Layer and the Upper SiO_2 Layer on the Guide Mode Properties

Our optimization process begins by studying the effect of the thicknesses of the Si layer and the upper SiO_2 layer on the performance of the device while keeping the dimension of the ridge ($h = 1000$ nm, $w = 1000$ nm) constant. The propagation length and mode effective index as a function of the thickness of the upper SiO_2 layer (t_2) for different initial thicknesses of Si layer (t_0) are shown in Fig. 2(d). As shown, the mode effective index decreases with the increase of t_2. As for the propagation length, there is an optimum thickness for which propagation length is maximized. We also note that for different initial thicknesses of Si layer (t_0) there is a different optimized thickness t_2 for which the largest propagation length is obtained. One can understand this observation as follows: the propagation length is in fact determined by the effective dielectric constants below and above the metal stripe, which can become similar and obtain the maximal propagation length by adjusting the thickness of upper layer SiO_2. In practice, the effective index of medium below the metal stripe consists of a weighted average of the Si and the SiO_2 layers, where the weights for each layer depends on the modal distribution within the layers. Therefore, the two parameters are related to each other. Fig. 2(a)–(c) shows the field distributions for different t_0 with optimized t_2 and indicates that the mode confinement at small t_0 is much better than at large t_0. For a small $t_0, t_0 = 200$ nm, the propagation length with optimized t_2 ($t_2 = 83$ nm) is 0.79 mm, and for a larger $t_0, t_0 = 300$ nm, the propagation length with optimized t_2

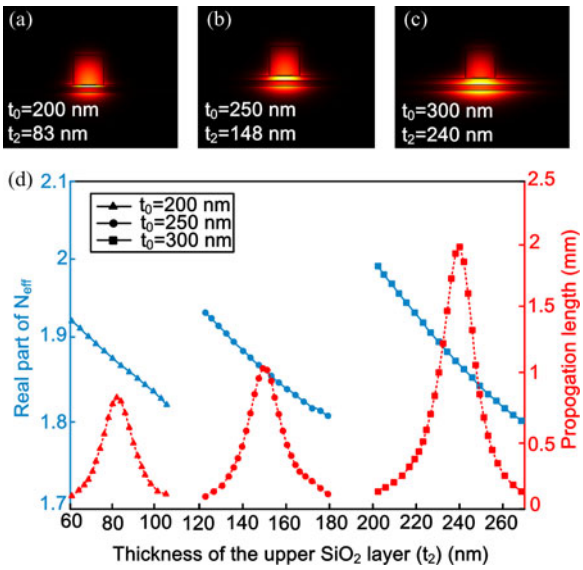

Fig. 2. (a)–(c) Field distribution of abs(Ez) in the cross section of the waveguide with different parameters; (a) $t_0 = 200$ nm, $t_2 = 83$ nm, propagation length $L_p = 0.79$ mm, (b) $t_0 = 250$ nm, $t_2 = 148$ nm, propagation length $L_p = 1.07$ mm, and (c) $t_0 = 300$ nm, $t_2 = 240$ nm, propagation length $L_p = 2.01$ mm. (d) Real part of the mode effective index (shown by the solid line) and the propagation length (shown by the dashed line) *versus* the thickness of the upper SiO_2 layer. The initial thicknesses of the Si layer are 200 nm, 250 nm and 300 nm, respectively.

($t_2 = 240$ nm) is 2.01 mm. The thickness of the Si layer mainly determines the mode confinement and the thickness of the upper SiO_2 layer mainly determines the propagation length. With the increase of t_0, the propagation length increases and the mode becomes less confined, thus having smaller interaction with the metal. This tradeoff between confinement and propagation loss is common to most of the plasmonic waveguides.

B. Influence of Different Materials of Metal Stripe on the Guide Mode Properties

In order to investigate the influence of different metal stripes, gold (Au) and aluminum (Al) are introduced to compare with copper. The refractive indices of the metals at 1.55 μm are taken from [29]. The initial thickness of Si layer is set at $t_0 = 250$ nm and the dimension of the ridge ($w = 1000$ nm, $h = 1000$ nm) is kept constant. The relationship between different materials of metal stripe and the propagation lengths are shown in Fig. 3. For Au ($n_{Au} = 0.55 + i11.5$) stripe which is incompatible with CMOS technology the largest propagation length of 1.92 mm is obtained, whereas for Al ($n_{Al} = 1.58 + i15.66$) stripe the shortest propagation length of 0.82 mm is observed. For Cu which is chosen as the metal stripe in the proposed structure propagation length of 1.07 mm is predicted. To be noted, the optimized thicknesses of upper SiO_2 layer (t_2) are almost the same for the three different metal stripes for the same t_0.

C. Influence of the Dimension of the Ridge on the Guide Mode Properties

Next, the dimensions of the ridge need to be optimized. The initial thickness of the Si layer is chosen at $t_0 = 250$ nm and we

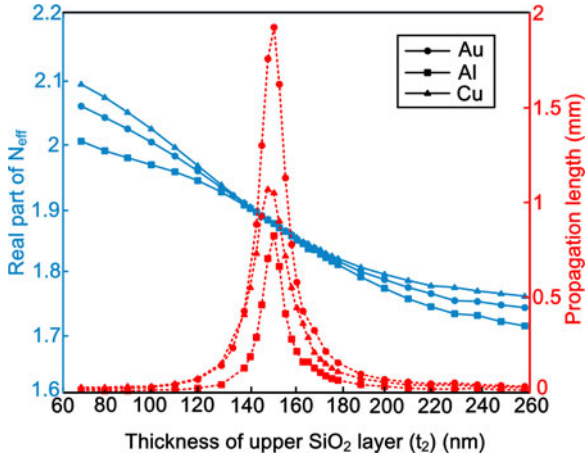

Fig. 3. Real part of the mode effective index shown by the (solid line) and the propagation length (shown by the dashed line) *versus* the thickness of the SiO_2 layer (t_2) oxidized from 250-nm Si layer for different materials of metal stripe. The materials of metal stripe are chosen as gold ($n_{Au} = 0.55 + i11.5$), copper ($n_{Cu} = 0.606 + i8.92$), and aluminum ($n_{Al} = 1.57851 + i15.658$), respectively.

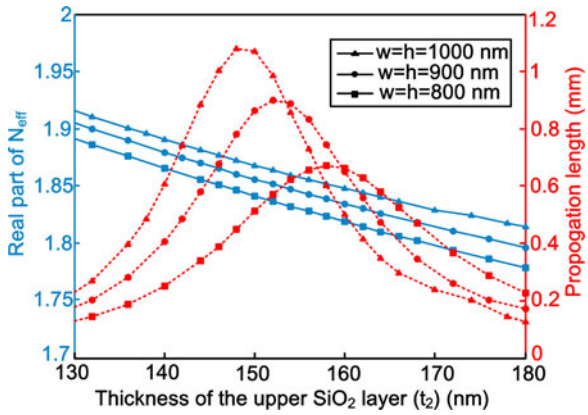

Fig. 4. Real part of the mode effective index (shown by the solid line) and the propagation length (shown by the dashed line) *versus* the thicknesses of the SiO_2 layer oxidized from the 250-nm Si layer. The dimensions of the ridges are 1000 nm × 1000 nm, 900 nm × 900 nm, and 800 nm × 800 nm, respectively.

calculate the effective index and the propagation length for three different dimensions of square ridges: 1000 nm × 1000 nm, 900 nm × 900 nm, and 800 nm × 800 nm. The results are shown in Fig. 4. With the decrease of the dimension from 1000 to 800 nm, the optimized thickness of upper SiO_2 layer (t_2) increases from 148 to 158 nm, while the effective mode index and the propagation length both show a decrease. The propagation lengths are 1.07, 0.9, and 0.67 mm for the 1000, 900, and 800 nm square ridges, respectively.

D. Influence of the Metal Stripe Width on the Guide Mode Properties

The long range SPPW guide mode consists of contributions from the opposite modes propagating along the finite metal stripe surface and proper choice of metal stripe width greatly affects the properties of this guided mode. Increasing the width of metal stripe weakens the coupling between the two opposite modes with the result of higher propagation loss. Fig. 5 shows

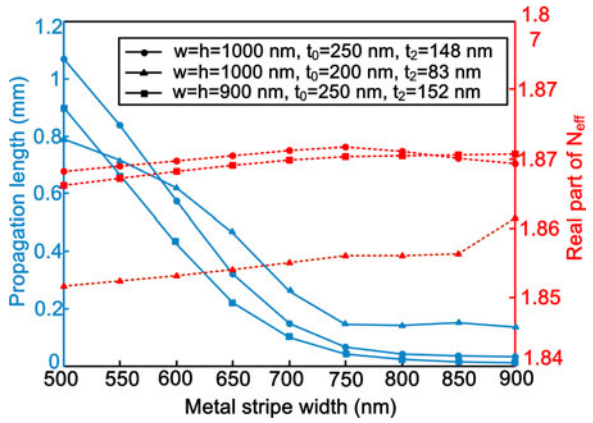

Fig. 5. The propagation length (shown by the solid line) and real part of the mode effective index (shown by the dashed line) *versus* copper stripe width for different dimensions of ridges and optimized t_2 with different t_0.

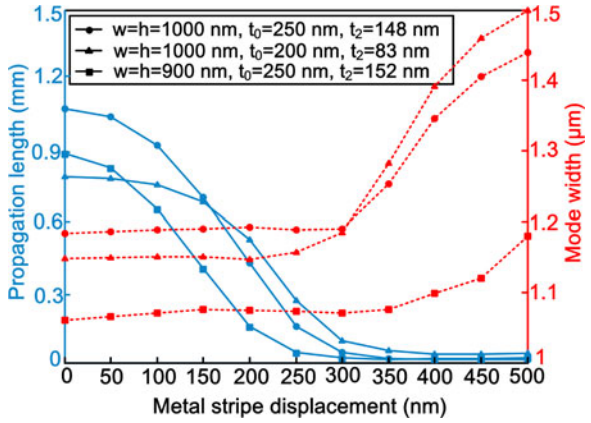

Fig. 6. The propagation length (shown by the solid line) and the lateral mode width (shown by the dashed line) *versus* the displacement of a 500-nm copper stripe for different dimensions of ridges and optimized t_2 with different t_0.

the propagation length and real part of the mode effective index as a function of the copper stripe width for different dimensions of ridges and optimized t_2 with different t_0. The dimensions of the ridges are 900 nm × 900 nm and 1000 nm × 1000 nm, and the thicknesses of the upper SiO_2 layers (t_2) are adjusted according to the ridge dimensions and t_0 for optimum propagation length. With an increase of the metal stripe width from 500 to around 750 nm, the coupling between the two opposite modes becomes negligible and the propagation length drops dramatically from millimeter range to micrometer range, while the mode effective index shows a slight increase. When the metal width is over 750 nm, there is no LR mode and only the standard single interface SPP mode existed on the dielectric–metal interface, which explains the short propagation length.

E. Influence of the Displacement of the Metal Stripe on the Guide Mode Properties

So far, the metal stripe is assumed to be placed symmetrically in the center of the ridge. However, in practice the metal stripe may be shifted from the center of the ridge due to misalignment in the fabrication process. We now analyze the influence of such a displacement on the guide mode properties. The displacement of the metal stripe introduced an asymmetry to the waveguide and perturbed the balance of the modes on the both sides of the metal stripe, with the result of additional propagation loss and larger mode width. Fig. 6 shows the propagation length and real part of the mode effective index as a function of the copper stripe displacement for three different dimensions of structures as mentioned above. Up to displacement of about 250 nm, mode is still confined in the ridge area and the mode varies very little. Meanwhile, the propagation length drops dramatically because of this asymmetry as a result of the stronger interaction with the metal. When the displacement is over 250 nm, the drop in propagation length is slowed down. For displacement larger than 300 nm, the mode width shows a rapid increase whereas the propagation length stays at a low level. For such a case the symmetry of the waveguide is completely destroyed and there is no LR mode propagating. Instead, the propagating

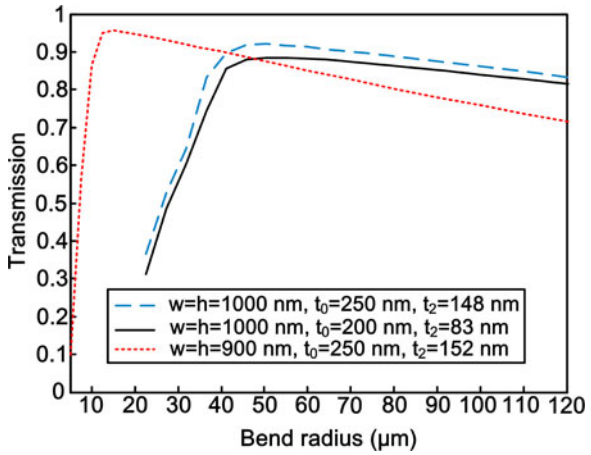

Fig. 7. The transmission of guide mode through a 90° circular bent proposed LR-DLSPPW *versus* the bend radius for different dimensions of ridges and optimized t_2 with different t_0.

mode is equivalent to a single interface SPP at the interface between the metal and SiO_2. It should be noted however, that up to misalignment of ∼100 nm, the drop in propagation loss is not drastic and propagation length of ∼0.65–0.95 mm are still achievable. With current technology, keeping the misalignment within 100 nm is definitely feasible.

F. Influence of the Bend Radius on the Transmission

To integrate the DLSPPW into plasmonic circuitry, the effect of waveguide bend must be addressed. To do so, the bend loss of the waveguide is calculated with conformal transformations through standard mode solvers implemented with FEM [33], [34]. Fig. 7 presents the transmission of the guide mode propagating through a 90° circular bent within the proposed LR-DLSPPW as a function of the bend radius for three different dimensions of structures as mentioned previously. The transmission first increases and then decreases as a function of the bend radius, showing that the overall loss is dominated by the bending loss at a small bend radius and by propagation loss at a large bend radius. The structure with the 900 nm ×

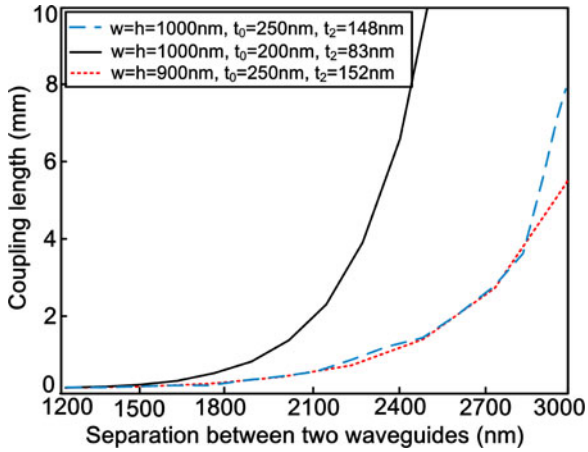

Fig. 8. The Coupling length of two parallel waveguides *versus* the separation distance for different dimensions of ridges and optimized t_2 with different t_0.

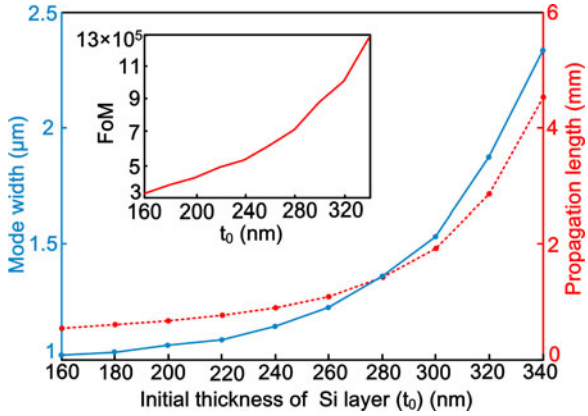

Fig. 9. Lateral mode width (shown by the solid line) and propagation length (shown by the dashed line) *versus* the initial thickness of the Si layer (t_0) with optimized t_2 for maximal propagation length. The dimension of the ridge is 1000 nm ×1000 nm and the inset shows the figure of merit as a function of t_0.

900 nm ridge obtains a transmission of 95% at a small optimal bend radius (R∼17 μm) whereas the other two structures with 1000 nm × 1000 nm ridges obtain the same optimal bend radius of R ∼ 45 μm. The two devices with similar ridge dimensions show very similar transmission for a broad range of bend radii, whereas the smaller ridge device can sustain much lower bend radius at the expense of higher propagation loss.

G. Coupling Length

When two waveguides are placed next to each other, mode overlap and energy coupling for the similar modes will happen, which can be defined as crosstalk. The crosstalk between two parallel waveguides determines how closely waveguides can be packed on a chip. The coupling length for which the energy is fully transferred between two parallel waveguides placed next to each other is determined by considering the mode effective index difference between symmetric mode and asymmetric mode [21]:

$$L_{\mathrm{coupl}} = \frac{\lambda}{2 \times (N_{\mathrm{sym}} - N_{\mathrm{asym}})} \tag{1}$$

where N_{sym} and N_{asym} are the mode effective indexes of the symmetric and asymmetric modes, respectively. With the increase of the center-to-center distance, when the coupling length is five times larger than the propagation length, the two waveguides can be considered isolated because the coupling from one waveguide to another is quite weak and can be neglected [29]. Fig. 8 shows the coupling length of two parallel waveguides as a function of the separation distance (center to center) for three different dimensions. The proposed three waveguides have different propagation lengths (0.79, 0.9, and 1.07 mm, respectively), which can be compared with their coupling lengths. For the waveguide with w=h = 1000 nm, t_0 = 200 nm, t_2 = 83 nm, a separation distance of 2300 nm obtains a coupling length of over 4 mm, which is over five times of the propagation length 0.79 mm and the isolation is guaranteed. The other two waveguides show the similar coupling length and the isolation of mode propagation can be ensured with a separation of 3000 nm. The proposed waveguides have much better safe separation distances than the similar LR-DLSPPW proposed in [21] and [35], which both have over 5000 nm isolation guaranteed separation distances. The coupling length is more likely to be determined by t_0, rather than by the ridge dimension, which is the opposite to the results of bend loss. In order to avoid the crosstalk and reduce the bend loss, a tradeoff should be made between the ridge dimension and t_0.

H. Figure of Merit

To evaluate the performance of a plasmonic waveguide in this design, propagation lengths and mode confinement (lateral mode width) should both be considered. Propagation length represents how long the mode can be transmitted and the lateral mode width determines the bend loss and coupling length, which are two essential properties in on-chip circuitry. As mentioned previously, there is a tradeoff between the propagation length and the lateral mode width. Fig. 9 shows the lateral mode width and the propagation length as a function of t_0 with a 1000 nm × 1000 nm ridge. For each value of t_0, t_2 is optimized for maximal propagation length. With an increase of t_0, both propagation length and lateral mode width are increased. In addition, by increasing the initial thickness of Si layer (t_0) from 160 to 340 nm, the propagation length can research to 4.43 mm with a lateral mode width of ∼2.32 μm. Figure of merit (FoM) which considers the lateral mode width w, as well as the propagation length L_p is introduced to evaluate the performance of waveguide [35]:

$$\mathrm{FoM} = L_p^2 \frac{\lambda}{n_{\mathrm{eff}}\, w^3}. \tag{2}$$

The inset of Fig. 9 shows the FoM as a function of t_0. Taking $t_0 = 250$ nm for example, the propagation length L_p is 1.07 mm and the mode width w is 1.18 μm, resulting in an FoM of 5.8 × 10^5. Such an FoM value is significantly higher than other kind of SPP waveguides mention in [35] and is comparable with the LR-DLSPPW which is incompatible with CMOS technology. With the advantages of the CMOS-compatible characteristics

and such a high FoM, the proposed waveguide structure is a good candidate for on-chip integrated plasmonic circuitry.

IV. Conclusion

In conclusion, a CMOS-compatible LR-DLSPPW designed to operate at telecom wavelengths with long propagation length and strong mode confinement has been proposed and numerically demonstrated using FEM simulations. The structure consists of a thin metal film embedded between a dielectric ridge made of silicon nitride (Si_3N_4) and two dielectric layers (Si and SiO_2) which are supported by a $\sim$2–3 μm SiO_2 layer on top of a silicon substrate. Proper choice of materials makes this structure compatible with CMOS microfabrication process. The dimensions of this six layer structure (Si_3N_4–Cu–SiO_2–Si–SiO_2-Substrate) are optimized and the performance shows a great promise for long range propagating with subwavelength dimension. The bend loss and coupling length are also calculated and it was shown that the bending loss can be reduced and the crosstalk can be avoided. With proper choice of parameters (e.g. $w = h = 1000$ nm, $t_0 = 250$ nm, $t_2 = 148$ nm), the propagation length exceeds 1.07 mm, and lateral mode confinement of 1.18 μm is achieved. By increasing the initial thickness of Si layer (t_0) to 340 nm, the propagation length can be increased to 4.43 mm with a lateral mode width of $\sim$2.32 μm. A figure of merit which takes into account both the propagation length and the lateral mode width is introduced to evaluate the performance of waveguide. The high FoM indicates that the proposed structure is promising in realizing CMOS-compatible active plasmonic components.

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