

# Non-Volatile Silicon Photonics Using Nanoscale Flash Memory Technology


Meir Grajower, Noa Mazurski, Joseph Shappir, and Uriel Levy\*

Nonvolatile flash memory technology is widely used in our daily life. Following the recent progress in silicon photonics, there is now an opportunity to embed flash memories also in photonic applications. As of today, chip scale photonic devices, e.g., micro-resonators, are becoming essential building blocks in modern silicon photonics. However, their properties, such as their resonance frequencies, fluctuate due to fabrication tolerances, significantly limiting their applicability. Here, by integrating the well-established non-volatile flash memory technology into silicon photonic circuitry, this major obstacle is tackled and electrical post trimming of such resonators is demonstrated. Specifically, the Metal-Oxide-Nitride-Oxide-Silicon (MONOS) structure is used to trap charges in the thin silicon nitride layer, located in close proximity to the silicon device layer. This enables accumulating charges in the silicon, modifying the effective index of the optical mode and consequently the resonance frequency. By doing so, a robust and CMOS compatible nonvolatile memory solution is provided, which not only allows for precise trimming of the resonance frequency of the photonic device, but can also be easily manufactured and commercialized. This approach paves the way for efficient utilization of photonic structures such as resonators and interferometers in chip scale silicon photonics and electro optic systems, with a wide range of applications spanning from filters, switches and modulators, to sensors, and even lasers.

## 1. Introduction

Silicon based nanophotonic devices such as interferometers and resonators are serving as important building blocks in modern chip scale photonic circuits, supporting diverse functionalities such as modulation, switching, filtering, wavelength selection and dispersion control, biochemical sensing and others.<sup>[1–13]</sup> The integration of silicon with advanced platforms such as conductive oxide, polymers and atomically thin two dimensional materials provides a route for even more advanced silicon based active nanophotonic devices.<sup>[14–20]</sup>

M. Grajower, N. Mazurski, Prof. J. Shappir, Prof. U. Levy  
Department of Applied Physics  
The Benin School of Engineering and Computer Science  
The Center for Nanoscience and Nanotechnology  
The Hebrew University of Jerusalem  
Jerusalem, 9190401, Israel  
E-mail: ulevy@mail.huji.ac.il

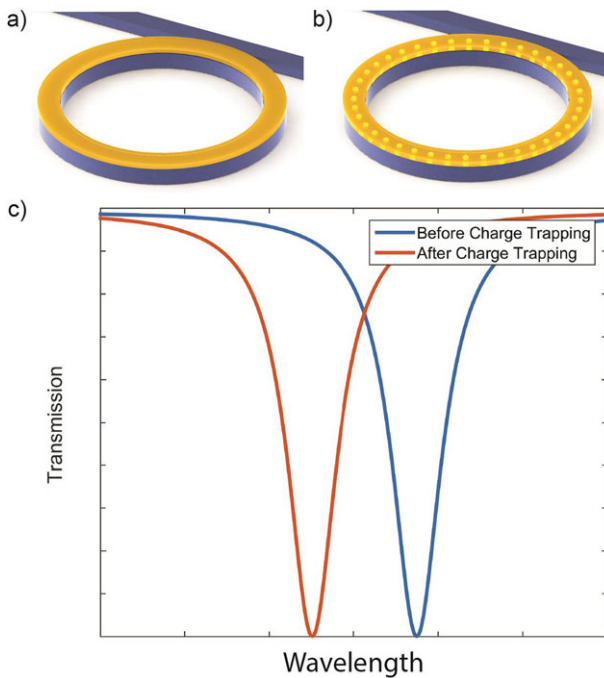
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A major challenge related to the practical implementation of nanophotonic resonators in chip scale optical communication systems is related to the accuracy in setting their resonance wavelength. For example, the actual resonance wavelength of two identical and adjacent resonators on the same chip can easily fluctuate in the range of about 10 GHz due to fabrication imperfections, (see e.g.<sup>[21]</sup>). Such fluctuations can be compensated by controlling the refractive index of the medium, either actively, e.g., by the use of the thermo optic effect,<sup>[7,22–24]</sup> or passively, by the use of post trimming approaches. Clearly, the thermo optic approach is far from being ideal as heating the structure requires significant electrical power. In addition, maintaining a constant difference in temperature between two adjacent resonators on a chip is challenging. Post processing trimming approaches which does not consume power are thus preferred. Indeed, several such approaches have been demonstrated, e.g., locally oxidizing the silicon surface or using phase change materials.<sup>[25–30]</sup> While these techniques

show promise due to the large achievable tunability (up to 20 nm), they are far from being CMOS compatible and they need non-standard setups for their implementation and activation. Essentially, there is still a strong need for a robust, reliable, accurate, reproducible and large scale CMOS compatible approach for the post trimming of silicon nanophotonic structures.

Hereby, we propose and experimentally demonstrate a novel solution for the post trimming of nanophotonic resonators in silicon, by integrating the well-established MONOS (Metal-Oxide-Nitride-Oxide-Silicon) non-volatile flash memory technology into the photonic chip.<sup>[31]</sup> The approach is based on the trapping of charges in a thin nanoscale layer of silicon nitride embedded between two silicon oxide layers. The device is operating as a MOS (Metal-Oxide-Semiconductor) capacitor, and the trapped charges modify the concentration of free carriers in the silicon device layer of an SOI (silicon on insulator) based nanoscale waveguides, which are used as the basic building block of chip scale photonic resonators. The end result is an **electrically controlled** memory which shifts the resonance frequency via the free carrier plasma dispersion effect. Our concept is schematically illustrated in **Figure 1**.



**Figure 1.** A schematic illustration demonstrating the trimming of the resonance frequency of chip scale silicon photonic resonators using charge trapping in a nanoscale nitride layer. a,b) Illustration of a micro-ring resonator (in blue) with nitride layer on top of it (in orange) without and with trapped charges in the nitride layer, respectively. Cross section of the structure is presented in Figure 2a. c) Schematic plot showing the shift in resonance frequency due to charge trapping in the nitride layer.

## 2. Fabrication

The device was fabricated on a commercial SOI wafer (SOITEC) with a  $2\ \mu\text{m}$  buried oxide layer and a  $220\text{nm}$  top silicon (Boron doped,  $N_a = 5 \times 10^{17}[\text{cm}^{-3}]$ ) layer. First, a passive structure was fabricated by a commercial fab (Towerjazz semiconductor Ltd.). This structure consists of the silicon waveguides implemented in a rib configuration with cross sectional dimensions of  $450\ \text{nm}$  width,  $220\ \text{nm}$  height and rib of  $80\text{nm}$  (Figure 2a). Two microring resonators (MRRs,  $30\ \mu\text{m}$  diameter each) were coupled to the bus waveguide in series, one after the other. Next, several steps were made in-house to make the active device. On top of the waveguide and MRR structures, three insulating layers were formed:  $8\text{nm}$  of silicon oxide by thermal oxidation,  $6\text{nm}$  of plasma enhanced chemical vapor deposition (PECVD) silicon nitride, and a  $\approx 500\ \text{nm}$  thick PECVD silicon oxide. On top of the thick oxide above the MRR, a  $150\ \text{nm}$  thick layer of aluminum (Al) was deposited using electron beam evaporation to form the gate of a MOS structure as shown in Figure 2. The Al layout above the two MRRs is not identical - above MRR C1 (Figure 2d), the Al contact pad area is small ( $\approx 10,000\ \mu\text{m}^2$ ) and only partially covers the silicon MRR. This aluminum is patterned as a periodic structure with a period of  $2\ \mu\text{m}$  and duty cycle of 0.5. These openings enable photo emission of electrons from the silicon using ultraviolet (UV) light source, as will be explained later. Above MRR C2 (Figure 2d), the Al covers the entire MRR with a larger contact pad area ( $\approx 50,000\ \mu\text{m}^2$ ). This large pad serves two purposes:

a) preventing photo emission by blocking the UV illumination, and b) eliminating the need to form ohmic contact to the silicon layer. Additional contact is made in the back side of the SOI wafer. The obtained structure is that of two Metal-Oxide-Semiconductor (MOS) capacitors connected in series with a silicon nitride layer sandwiched between the two silicon oxide layers near the silicon in both capacitors, forming an oxide-nitride-oxide (ONO) structure. The two capacitors configuration enables the measurement of the device without making a direct electrical contact to the top silicon waveguide layer which was avoided for reasons of process simplicity.

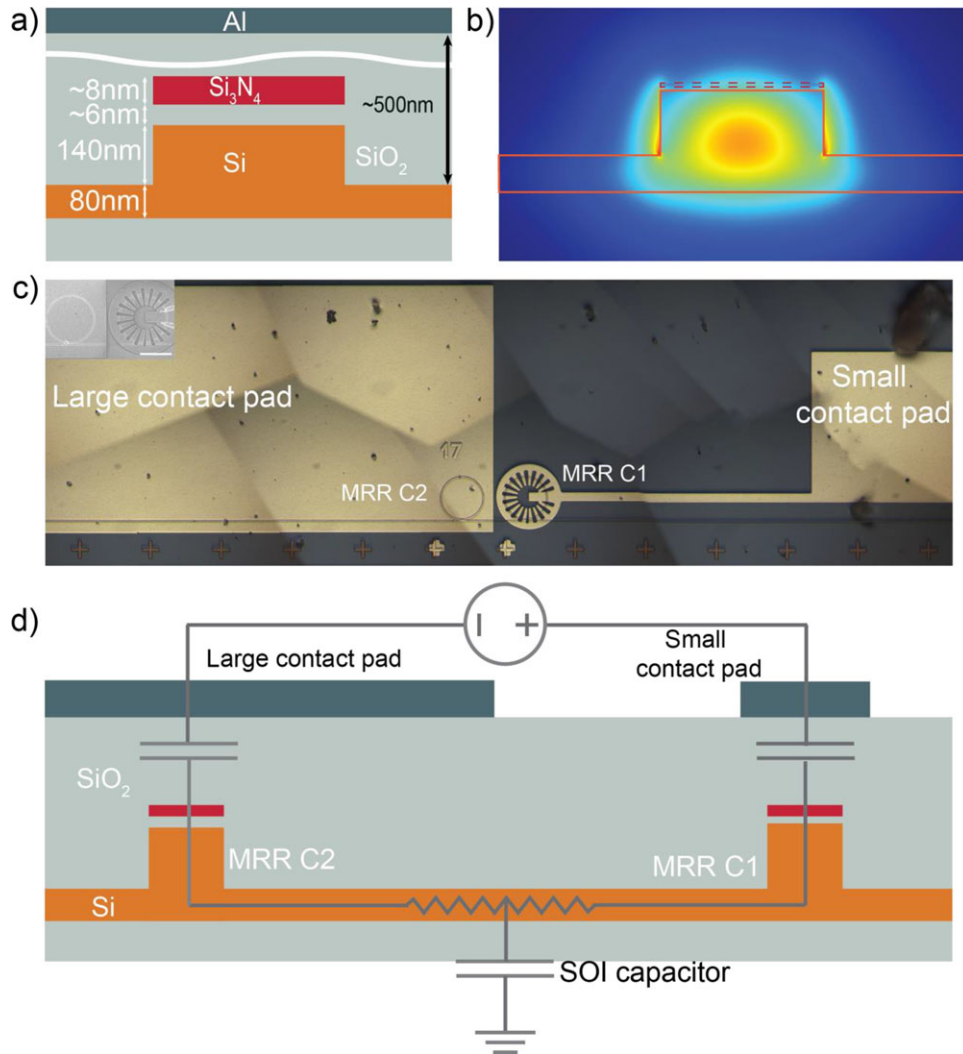
## 3. Concept of Operation

As mentioned before, the motivation of this work is to introduce an electrical post processing method of controlling the resonance frequency of the MRR. This goal is achieved by using the concept of the MONOS\SONOS (MONOS is identical to SONOS, with the exception of replacing the poly gate by a metal gate) flash memory.<sup>[31,32]</sup> In short, MONOS\SONOS allows the injection of controlled amount of electrons into the nitride layer. These charges induce opposite charges in the silicon near the silicon-oxide interface and allow to drive the MOS capacitor into accumulation, depletion, and even inversion mode. Furthermore, the trapped charges are stable and can be kept for long time ( $>10$  years).<sup>[33,34]</sup> Moreover, high stability of several years should be maintained even for higher temperatures, up to  $\approx 100$  degrees centigrade, as in SONOS based flash memory technology.<sup>[35]</sup> While in flash memory applications the readout of memory is achieved by measuring electrical parameters such as voltage or current, here we use optical readout instead. The induced change in the density of free carriers results in a change in the effective refractive index of the MRR via the free carrier plasma dispersion effect.<sup>[36]</sup> As a result, the resonance frequency varies as well following the relation:

$$2\pi r n_{eff} = m\lambda \quad (1)$$

At this point, it is helpful to review the basic physical concepts underlying the operation of the MONOS\SONOS flash memory. Upon the application of positive voltage to the gate electrode of the device, electrons tunnel from the silicon through the oxide into the nitride layer. The relatively thin layers used in commercial SONOS based devices enable the electron tunneling at relatively low voltages. The gate electrode, which is about  $\approx 20\ \text{nm}$  away from the silicon, can be used both for the tunneling process as well as for the measurement of the amount of trapped charges.

For optical applications, the above mentioned thickness of the MOS insulating layer of about  $20\ \text{nm}$  is not sufficient due to the ohmic loss in the metal. To avoid excessive optical loss, the thickness of the top oxide layer above the nitride layer was increased to  $\approx 500\ \text{nm}$ . This allows to minimize the effect of the Al gate layer on the loss of the waveguide mode, and thus avoiding a drastic reduction in the quality factor of the MRR. On the downside, the direct impact of increasing the thickness of the oxide layer is the need for operating at higher voltage during the charge trapping\detraping. To avoid breakdown of the oxide layer (which unavoidably, at this relatively large



**Figure 2.** a) schematic cross section of the silicon waveguide with the oxide-nitride oxide and the metal electrode layers on top. The Al contact on the back side of the SOI is not illustrated. b) cross section showing the electric field intensity of the transverse electric (TE-like) optical mode supported by the waveguide. The orange line bounds the silicon region, whereas the dashed red line represents the nitride layer. c) Panoramic microscope image of the waveguide and the two MRRs. The bright color corresponds to the Al. The waveguide and the MRRs can be clearly observed. d) Electrical scheme of the two MRRs and Al contacts, superimposed on the structure. The silicon rib between the two MRRs is modeled as a resistor. The SOI capacitor is huge compared to the two MRR capacitors. The MRR C1 is only partially covered by Al to enable exposure to UV light, while the MRR C2 is fully covered by a large Al electrode to prevent any light exposure. Furthermore, the circuit configuration 2d, allows the application of external voltage to MRR C1 without needing an ohmic contact to the silicon layer. All panels are sketched not to scale.

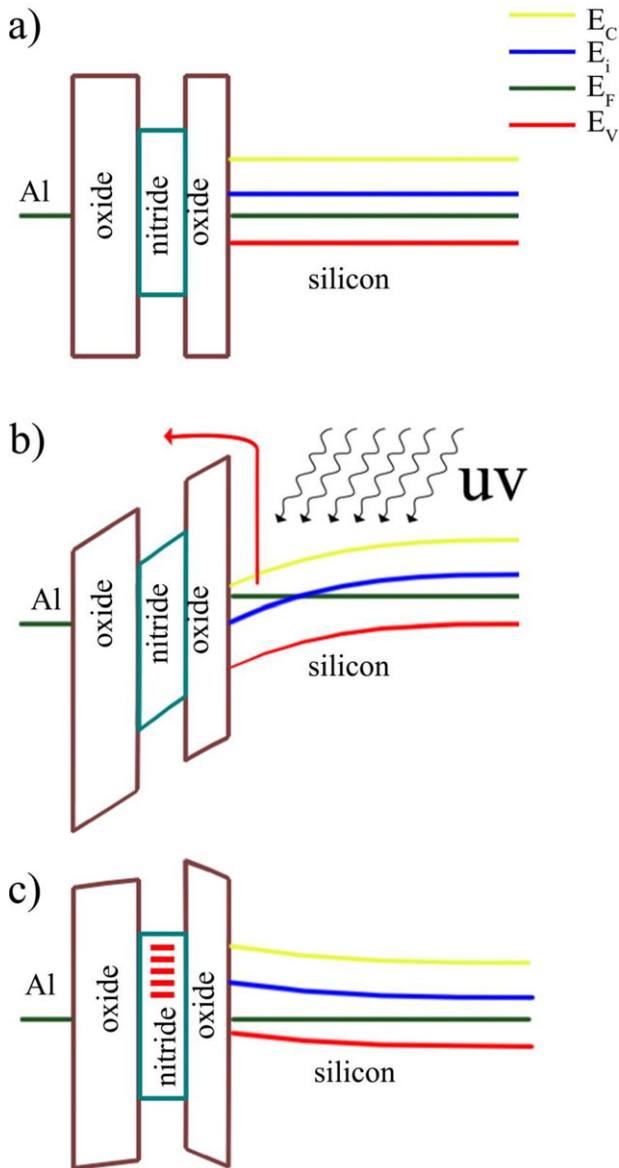
thickness contains some defects), we replaced the tunneling process by internal photo emission as the method of injecting electrons into the nitride layer. The process is shown schematically in **Figure 3**.

### 3.1. Charge Trapping

Unlike tunneling injection from the silicon conduction band (as in the typical Flash memory), in our case of internal photo emission the electrons are injected from the silicon valence band. This is due to the low probability of the photo emission process of electrons from the conduction band which is very lightly populated as a result of using p-type layer. The potential barrier between

the silicon valence band and the silicon oxide conduction band is 4.3 eV. This high energy is supplied by a UV light emitting diode with center wavelength around 250 nm (4.96 eV).

To ensure that the UV illumination penetrates all the way to the silicon, we replaced the continuous metal electrode above the MRR by a comb-like structure. The amount of trapped electrons is determined by the applied positive gate voltage. The photo excited electrons at the silicon surface layer are carried towards the nitride layer by the electric field of the applied gate voltage. This charge injection is a self-stopping process as the trapped electrons induce an opposite electric field with increasing strength which is directly proportional to the trapped charge density. This increasing field reaches a value which compensates the gate induced electric field to the point that photo induced electron



**Figure 3.** Schematic illustration of the charge trapping mechanism in our device (not to scale). a) Flat band, i.e., no band bending. b) Electron photo emission – achieved by a combination of UV illumination and the application of positive voltage. The red arrow denotes the photoemission of electrons from the valence band of the silicon into the silicon nitride. c) The band diagram after electrons are trapped in the nitride and without the application of external voltage. The electrons in the nitride (shown as red bars) attract holes from the silicon-oxide interface, and the capacitor is found in accumulation mode.

injection is stopped. Thus, the saturation level of the injected electrons is determined by the value of applied gate voltage.

### 3.2. Optical Effect of the Trapping

Once the desired amount of trapped electrons is reached, the gate voltage is removed. The trapped charges are now neutralized by

opposite charges divided between the two electrodes of the MOS capacitor. Yet, considering the fact that the silicon electrode is located only 8 nm away of the nitride, whereas the metal gate is separated by a large distance of  $\approx 500$  nm, in practice all the compensating positive charge is located in the silicon.

The compensating charge is induced either by generating an accumulation layer at the interface (for p-type silicon, as in our device) or by depleting free carriers (in the case of n-type silicon). The change in free carrier concentration induces local change in the refractive index of silicon according to:<sup>[36]</sup>

$$\Delta n = - (8.8 \times 10^{-4} \Delta N_n + 8.5 \Delta N_h^{0.8}) \cdot 10^{-18} \quad (2)$$

where  $\Delta N_n$  is the change in electron concentration, and  $\Delta N_h$  is the change in hole concentration. Here, we have used a p-type silicon waveguide. As a result, an accumulation layer is generated at the interface between the silicon and the oxide layer, inducing a local change in the refractive index which in turn controls the resonance frequency of the MRR.

As shown in Figure 2, the device is constructed of two MRRs electrically connected in series. MRR C1 (Figure 2c,d) has a much smaller capacitance relative to MRR C2. Thus, the applied voltage on the two MOS capacitors in series falls mostly on C1, and the trapped charges are located on top of MRR C1. The end result is that MRR C2 serves as reference which allows to directly and accurately measure the resonance shift of MRR C1 by eliminating environmental effects such as thermal fluctuations which are identical for both MRRs. In addition, this configuration eliminates the need for ohmic contact to the silicon. Two-MRR configuration was recently used for the purpose of ultraprecise sensing.<sup>[21]</sup>

## 4. Results

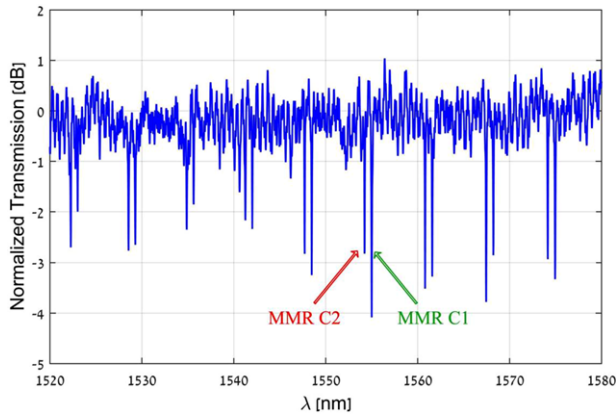
### 4.1. Experimental Setup

The measurement setup consists of a tunable laser source (Agilent 81640A) that is coupled in and out of the device using lensed fibers in a butt coupling configuration. The transmission of the device is measured as a function of wavelength. In addition, a variable DC power supply (SRS PS310) is connected to two probes which apply voltage on the MRRs (connected to gate of MRR C1 and MRR C2, Figure 2c,d). The gate electrode of MRR C2 (large area) together with the back side of the SOI are connected to the ground potential. The voltage is applied to the gate metal of MRR C1. As mentioned, based on the difference in the capacitance of C1 and C2, practically almost all the voltage is applied to MRR C1.

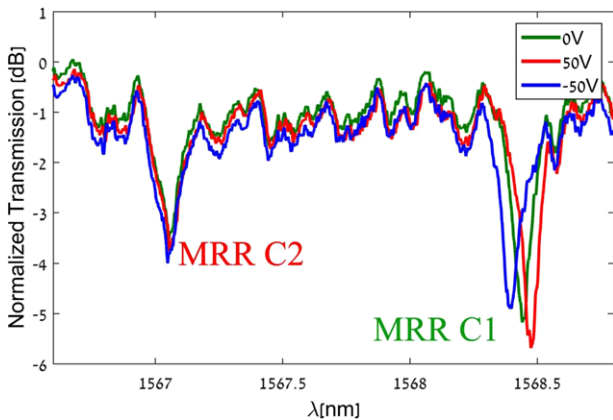
Electrons are photo injected from the silicon into the nitride layer by UV illumination (UV LED, Thorlabs E250) where positive DC voltage is applied on the gate of MRR C1.

### 4.2. Experimental Results

The two MRRs are fabricated with the same dimensions, and are thus expected to have the same optical behavior. However, it is well-known that local minor variations in the fabrication process



**Figure 4.** Normalized transmission spectrum of the device. Even though the parameters of the two MRRs are identical, two different resonance frequencies corresponding to the two MRR are evident.

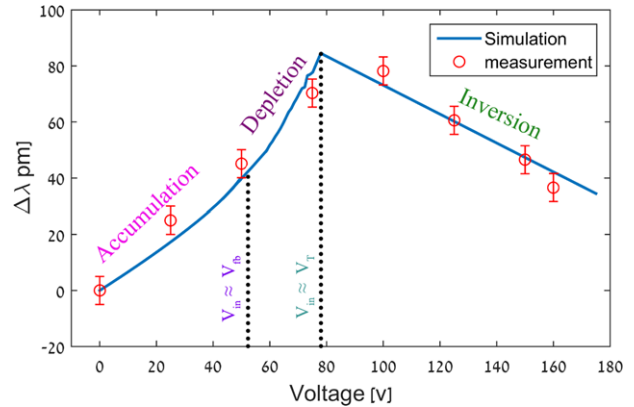


**Figure 5.** Normalized transmission spectrum of the device measured under three different applied voltages. As expected, under positive voltage the spectrum is red shifted while under negative applied voltage it is a blue shifted.

parameters lead to variations in the resonance frequency, typically in the range of tens of gigahertz.<sup>[21]</sup> Furthermore, some our post processing steps led to even larger detuning. Indeed, the measured transmission spectrum (**Figure 4**) shows clear traces of two resonances originating from the two MRRs which are slightly detuned.

Next, the devices were tested for their response to variable gate voltages, without the application of UV light, so that charge trapping is still deactivated. The effect of positive and negative gate voltages is shown in **Figure 5** where we limit the wavelength scan to two adjacent resonances.

As observed from **Figure 5** (right resonance, MRR C1), blue shift is obtained for negative voltage while red shift is obtained for positive voltage. This is expected, because for negative voltage holes are accumulated, reducing the effective refractive index, whereas for positive voltage the holes are depleted and the effective refractive index is increased. It is also clear from **Figure 5** that the left side resonance shows no shift under applied bias, and is therefore attributed to MRR C2, while the right resonance corresponds to MRR C1 (as shown by the arrows in **Figure 4**). It should be noted that after the voltage was set back to zero, the resonance



**Figure 6.** Simulation results (blue line) and experimental measurements (red circles) showing the shift between the resonance frequencies of the two MRRs under different applied voltage. The resonance frequency shift at 0 V is arbitrarily set to 0. Also indicated are the different regimes of the silicon band bending.

frequency returned to its initial value, i.e., to its value prior to the application of voltage. This indicates that any charge shift, either by tunneling or by other mechanisms (e.g., Poole-Frenkel) is insignificant in our system.

Typically, a MOS capacitor is not in a flat band condition under zero applied bias. This is because of the initial difference in work function between the metal and the silicon, as well as due to residual trapped charges in the dielectric layer during the fabrication process. As a result, an initial band bending is expected. In order to characterize the band bending, we repeated the experiment presented in **Figure 5**, by performing spectral measurement under different positive voltage bias, this time with smaller voltage steps, and extracted the resonance shift at each applied voltage. The obtained results are shown in **Figure 6** (red curve). In addition, the expected resonance shift was calculated (blue curve) using finite element solver (FEM, COMSOL Ltd., see supplementary). To fit the calculations to the experimental results, the following procedure was adopted. First, the resonance shift was divided by 1.8. This can be explained by the fact that the model assumes uniform voltage across the MRR whereas in practice the metal gate is patterned (in a fingers shape) and covers only 50% of the MRR area. Given the fact that the fingers width and spacing of the gate metal are twice the thickness of the gate oxide so that the effect of fringing fields cannot be ignored.

Next, to fit the voltage axis of the simulation to the measured data, two parameters were used - shift and scaling. The shift is attribute to the initially trapped charges in the oxide and nitride (as mentions before), while the scaling is attribute to variation of the oxide thickness and dielectric constant.<sup>[37]</sup>

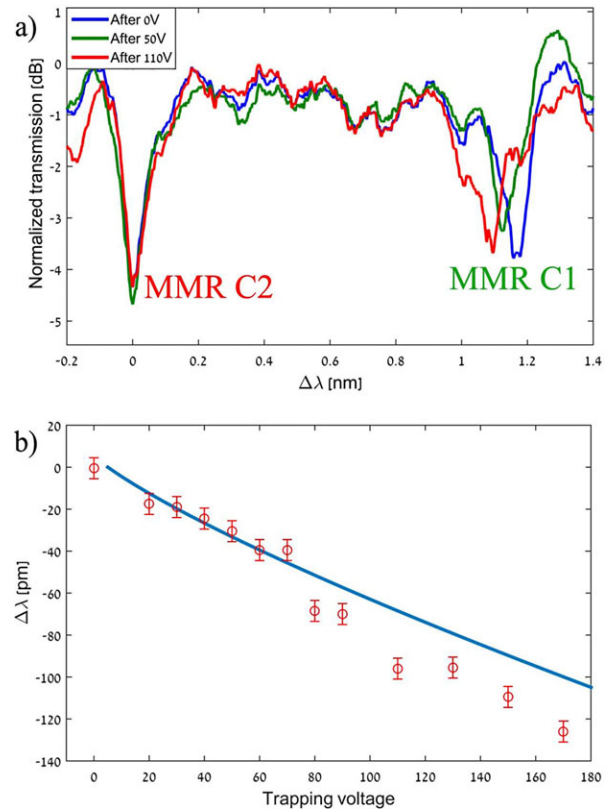
From the shape of the curves and from extracting these fitting parameters, it can be understood that at zero gate voltage there is already an accumulation layer at the silicon surface. As the voltage is increased, the accumulation layer is diminished and flat band condition is achieved. Further increase in applied voltage induces the formation of a depletion layer which reaches its maximum at a gate voltage of about 80 V. As the gate voltage increases beyond  $\approx 80$  V, the resonance frequency shift is decreased, indicating that an inversion layer is formed. Therefore, the

flatband voltage can be calculated by:  $V_{FB} = V_G - V_T = 80 - V_T = 80 - (2\phi_F + \frac{Q_d}{C_{ox}})$ , where  $V_{FB}$  is the flat band voltage,  $\phi_F$  is the Fermi energy,  $Q_d$  is the depletion charge,  $C_{ox}$  is the thick oxide capacitance and  $V_T$  is the threshold voltage for inversion. Using this relation, the flatband voltage is estimated to be  $\approx 45$  V. The relatively high values of  $V_T$  as compared to standard MOS devices is attributed to the thick gate oxide as well as to the trapped charges in the nitride layer as it comes out of the fabrication process.

Following the characterization of our device as a MOS capacitor, we turn into demonstrating the major goal of this paper, namely the possibility of obtaining permanent and controlled shift of the resonance wavelength by charge trapping in the thin nitride layer embedded within the MOS dielectric as is commonly done in Flash memories. As previously mentioned, we increased the total dielectric thickness from  $\approx 30$  nm to nearly 500 nm in order to reduce the propagation loss of the optical mode which results in from the ohmic loss in the metal. Such a thick oxide, which is deposited using PECVD, is exposed to defects and cannot sustain high electric fields. As a result, the overall voltage that can be applied is limited by the breakdown of the thick oxide, effectively limiting the electric field that can be applied to the thin tunneling oxide layer separating the silicon from the silicon nitride layer. This prevented us from using tunneling effect to transfer electrons from the silicon into the nitride layer. To overcome this obstacle, we choose the use of internal photo emission, i.e., UV assisted transfer of electrons from the valance band of the silicon to the silicon nitride layer.

Similar to the influence of the gate voltage on the resonance position (Figures 5 and 6), **Figure 7a** demonstrates the effect of the trapped charge in the nitride on the resonance frequency. Unlike the previous case, here the device was measured at zero gate voltage, after injecting charges at three different gate voltages. As can be seen, a noticeable trapping effect is observed. To better quantify this effect, we have repeated the charge trapping at many gate voltages. After each trapping procedure we measured the transmission spectrum of the device at zero gate voltage and extracted the resonance shift for each of the trapping events. The quantitative dependence of the resonance shifts on the trapped charges which are expressed through the gate voltage during the photo emission step is shown in **Figure 7b** (red circles). We have applied an increasing voltage of up to 170 V. When we further increased the voltage, an electrical breakdown occurred (See supporting Information S2). Finally, we calculated the shift of each trapping event (blue curve), using the same fitting parameters as in **Figure 6**.

As previously mentioned, the shift of the resonance frequency is dependent of the applied gate voltage as follow. The maximal charge that can be trapped in the nitride is estimated by  $Q_{max} = C_{ox} V_G$  (where  $V_G$  is the gate voltage and  $C_{ox}$  is the thick oxide capacitance). After the trapping event, the gate voltage is removed and the trapped charges induce an effective gate voltage in the silicon. The effective voltage is found to be  $V_{eff} = Q_{max} / C_{ono}$  where  $C_{ono}$  the capacitance of the thin oxide layer separating the nitride from the silicon. In our case, the effective voltage can be found to be  $V_{eff} = V_G \frac{C_{ox}}{C_{ono}} \approx \frac{V_G}{65}$ . Thus, the maximal effective field is the range of  $\approx 0.3$  volt per nanometer, which is the same order of magnitude as demonstrated in accumulation-based silicon photonic modulators.<sup>[38]</sup> For such a field strength in the trap-

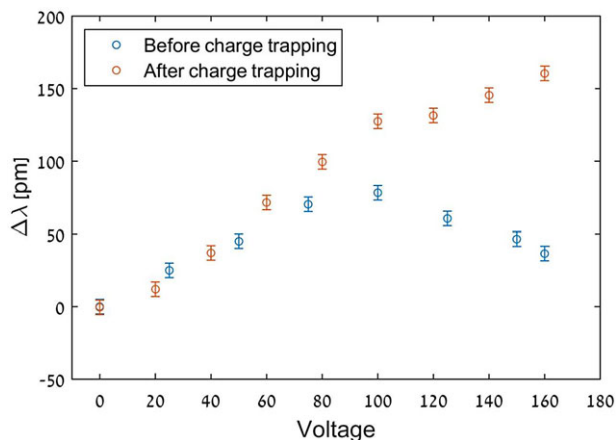


**Figure 7.** Experimental measurement demonstrating the effect of the trapped charge in the nitride layer on the resonance frequency of the MRR. a) Transmission spectrum measured at 0 V after UV illumination at three different gate voltages b) Resonance shift measured (red circles) and calculated (blue line) at 0 V after UV illumination under increasing applied gate voltages.

ping process we obtained a resonance shift of about 125 pm. This value can be further increased, e.g., by using a polysilicon electrode separated from the nitride by a high quality oxide layer which will allow both applying stronger fields, up to the breakdown field ( $\approx 1$  volt per nm), and also reducing the operation voltage for the trapping procedure. Such an approach may also allow to work in tunneling mode. This will enable not only trapping, but also the opposite action, i.e., erasing the trapping by applying an opposite voltage.

So far, we have shown separately the effect of gate voltage and trapped charge on the resonance shift. Next, we present the cumulative effect of the trapped charge under the application of a gate voltage. In **Figure 8** we show the resonance shift for different gate voltages after significant charge trapping at 160 V (red circles). For comparison, we also show the resonance shift of the same device at the same gate voltage prior to the charge trapping process (blue circles) before charge trapping (as in **Figure 6**). For simplicity, the initial frequency shift between the two MRRs is defined as zero in both cases, even though the shift is obviously different due to the trapping process (see **Figure 7b**).

As can be observed, in the case where no intentional charge trapping is applied, the threshold voltage,  $V_T$ , is achieved when the charge in the MOS capacitor compensates the initial charges in the nitride (which is typically fabrication process dependent)



**Figure 8.** Measurement of the resonance shift due to applied gate voltage after charge trapping (red circles). For comparison we show the results before charge trapping, as was also presented in Figure 5 (blue circles). For simplicity, the resonance shift between the two MRRs at zero gate voltage is set to zero in both cases, even though the shift is different due to the trapping operation.

and in the depletion layer. A voltage of  $\approx 80$  V is needed to achieve this condition. However, in the case where we intentionally trapped charges (red circles), the additional negative trapped charge injected into the nitride at  $V_G = 160$  V result in a significant increase in the total negative charge trapped in the nitride up to the point where even a gate voltage as high as 160 V is not sufficient to compensate the negative charge in the nitride and in the depletion region. Consequently,  $V_T$  is not reached, and a major difference in operation conditions between the pre-trapped and the post trapped cases is obtained.

## 5. Discussion and Conclusions

In conclusion, we have integrated a MONOS based non-volatile flash memory technology into photonic circuitry and utilized this structure to demonstrate a novel method of post resonance trimming of microresonators in a silicon photonics platform. With this process a resonance shift of up to about 125 pm was demonstrated. Our approach is based on the controlled injection of electrons into a nanoscale nitride layer bounded between two oxide layers in the insulating layer of MOS structure. As of today, the non-volatile flash memory is commonly used and it is being manufactured in high volumes at low cost. Thus, the proposed approach allows easy fabrication in a commercial CMOS fab and offers high reliability over time. Indeed, we have observed a stable charge trapping with no noticeable variations in resonance shift over the course of few weeks, and based on its proven reliability it is expected that undesired degradation in trimming capability will not be observed even at longer time duration of few years.<sup>[33,34]</sup> Based on the number of trapped charges and the intensity of our UV light source we estimate the time constant for trapping to be in the millisecond range.

The demonstrated concept can readily be used for overcoming unavoidable limited fabrication tolerances in a silicon photonics fab and to align the resonance frequencies of chip scale photonic resonators on demand. While we have demonstrated

the use of this method in microring resonators (MRR), this approach of using non-volatile flash memory for achieving a controllable and permanent change of the refractive index of silicon, can be implemented also in other photonic configurations such as photonic crystals, Mach Zehnder interferometers, Bragg gratings and other photonic devices operating on the basis of resonance or interference effect.

The demonstrated maximum shift in resonance wavelength of about  $\Delta \lambda_{max} = 125$  [pm] is already a significant landmark as it is typical of the fluctuations in resonance frequency between various resonators on the same chip, driven by slight variations in manufacturing. Yet, it should be possible to increase the tunability even further. For example, we can replace the MOS capacitor described here by full n-channel MOS transistor, enabling the operation in deep depletion mode. This way, the depletion layer could extend beyond the center of the optical mode, due to reverse bias of the n-type source and drain with respect to the p substrate. Under such a scenario, one may choose a silicon device layer with higher p-type doping of about  $\sim 7 \times 10^{17}$  [cm<sup>-3</sup>] to increase the free carrier plasma effect. We can also replace the top metal electrode by a lower loss, lightly doped ( $\sim 1 \times 10^{18}$  [cm<sup>-3</sup>]) polysilicon layer. This way, the oxide thickness can be significantly reduced. This will also enable the use of direct tunneling at much lower voltage and eliminate the need for UV based photoemission process.

The cumulative effect of this suggested structure is expected to allow much higher spectral tunability by the trimming process, towards  $\approx 1$  nm ( $\approx 120$  GHz) which is well above the typical variations in resonance frequency of identical MRRs. If such a device is implemented as a Mach Zehnder interferometer, it will reduce the length needed for achieving a  $\pi$  phase shift from about 3.8 mm to below half a millimeter.

The above mentioned improvements may also allow the erasing of charges, paving the way for extending the functionality of the device. For example, devices such as CMOS compatible electrically write – optically read memories could be implemented, offering a competitive alternative to previously reported non CMOS compatible approaches such as plasmonic memristors and others.<sup>[39–41]</sup> For such a device, a precise calibration of the detuning can be achieved by applying short voltage pulses together with monitoring the threshold voltage shift of the MOS transistor which should be added for the purpose of deep depletion. We estimate that such a calibration will allow a detuning precision of several MHz. The wealth of potential applications, combined with the ease of fabrication and the high potential for commercialization makes the integration of the MONOS\SONOS non-volatile flash memory technology into silicon photonics circuitry a particularly promising approach for the future development of silicon photonics.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

non-volatile memory, resonance trimming, silicon photonics

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