Optimization of efficiency-loss figure of merit in carrier-depletion silicon Mach-Zehnder optical modulator

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Abstract: In this paper we study the optimization of interleaved Mach-Zehnder silicon carrier depletion electro-optic modulator. Following the simulation results we demonstrate a phase shifter with the lowest figure of merit (modulation efficiency multiplied by the loss per unit length) 6.7V-dB. This result was achieved by reducing the junction width to 200 nm along the phase-shifter and optimizing the doping levels of the PN junction for operation in nearly fully depleted mode. The demonstrated low FOM is the result of both low $V_{\pi}L$ of ~0.78 Vcm (at reverse bias of 1V), and low free carrier loss (~6.6 dB/cm for zero bias). Our simulation results indicate that additional improvement in performance may be achieved by further reducing the junction width followed by increasing the doping levels.

OCIS codes (130.0250) Optoelectronics; (250.7360) Waveguide modulator; (250.5300) Photonic integrated circuits.

References and links

1. R. A. Soref and B. R. Bennett, "Electrooptical effects in silicon," IEEE J. Quantum Electron. **23**(1), 123–129 (1987).
2. L. Alloatti, D. Korn, R. Palmer, D. Hillerkuss, J. Li, A. Barklund, R. Dinu, J. Wieland, M. Fournier, J. Fedeli, H. Yu, W. Bogaerts, P. Dumon, R. Baets, C. Koos, W. Freude, and J. Leuthold, "42.7 Gbit/s electro-optic modulator in silicon technology," Opt. Express **19**(12), 11841–11851 (2011).
3. J. Liu, M. Beals, A. Pomerene, S. Bernardis, R. Sun, J. Cheng, L. C. Kimerling, and J. Michel, "Waveguide-integrated, ultralow-energy GeSi electro-absorption modulators," Nat. Photonics **2**(7), 433–437 (2008).
4. N. N. Feng, D. Feng, S. Liao, X. Wang, P. Dong, H. Liang, C. C. Kung, W. Qian, J. Fong, R. Shafiiha, Y. Luo, J. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "30GHz Ge electro-absorption modulator integrated with 3 μm silicon-on-insulator waveguide," Opt. Express **19**(8), 7062–7067 (2011).
5. G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, "Silicon optical modulators," Nat. Photonics **4**(8), 518–526 (2010).
6. Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," Nature **435**(7040), 325–327 (2005).
7. W. M. Green, M. J. Rooks, L. Sekaric, and Y. A. Vlasov, "Ultra-compact, low RF power, 10 Gb/s silicon Mach-Zehnder modulator," Opt. Express **15**(25), 17106–17113 (2007).
8. H. C. Nguyen, Y. Sakai, M. Shinkawa, N. Ishikura, and T. Baba, "10 gb/s operation of photonic crystal silicon optical modulators," Opt. Express **19**(14), 13000–13007 (2011).
9. A. Liu, L. Liao, D. Rubin, H. Nguyen, B. Ciftcioglu, Y. Chetrit, N. Izhaky, and M. Paniccia, "High-speed optical modulation based on carrier depletion in a silicon waveguide," Opt. Express **15**(2), 660–668 (2007).
10. P. Dong, S. Liao, D. Feng, H. Liang, D. Zheng, R. Shafiiha, C.-C. Kung, W. Qian, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Low Vpp, ultralow-energy, compact, high-speed silicon electro-optic modulator," Opt. Express **17**(25), 22484–22490 (2009).
11. N.-N. Feng, S. Liao, D. Feng, P. Dong, D. Zheng, H. Liang, R. Shafiiha, G. Li, J. E. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "High speed carrier-depletion modulators with 1.4V-cm VπL integrated on 0.25microm silicon-on-insulator waveguides," Opt. Express **18**(8), 7994–7999 (2010).

#192248 - $15.00 USD Received 14 Jun 2013; revised 27 Jul 2013; accepted 29 Jul 2013; published 12 Aug 2013

12. D. J. Thomson, F. Y. Gardes, Y. Hu, G. Mashanovich, M. Fournier, P. Grosse, J. M. Fedeli, and G. T. Reed, "High contrast 40Gbit/s optical modulation in silicon," Opt. Express **19**(12), 11507–11516 (2011).
13. J. Ding, H. Chen, L. Yang, L. Zhang, R. Ji, Y. Tian, W. Zhu, Y. Lu, P. Zhou, R. Min, and M. Yu, "Ultra-low-power carrier-depletion Mach-Zehnder silicon optical modulator," Opt. Express **20**(7), 7081–7087 (2012).
14. H. Yu, M. Pantouvaki, J. Van Campenhout, D. Korn, K. Komorowska, P. Dumon, Y. Li, P. Verheyen, P. Absil, L. Alloatti, D. Hillerkuss, J. Leuthold, R. Baets, and W. Bogaerts, "Performance tradeoff between lateral and interdigitated doping patterns for high speed carrier-depletion based silicon modulators," Opt. Express **20**(12), 12926–12938 (2012).
15. Z.-Y. Li, D.-X. Xu, W. R. McKinnon, S. Janz, J. H. Schmid, P. Cheben, and J.-Z. Yu, "Silicon waveguide modulator based on carrier depletion in periodically interleaved PN junctions," Opt. Express **17**(18), 15947–15958 (2009).
16. M. Ziebell, D. Marris-Morini, G. Rasigade, P. Crozat, J.-M. Fédéli, P. Grosse, E. Cassan, and L. Vivien, "Ten gbit/s ring resonator silicon modulator based on interdigitated PN junctions," Opt. Express **19**(15), 14690–14695 (2011).
17. H. Xu, X. Xiao, X. Li, Y. Hu, Z. Li, T. Chu, Y. Yu, and J. Yu, "High speed silicon Mach-Zehnder modulator based on interleaved PN junctions," Opt. Express **20**(14), 15093–15099 (2012).
18. J. C. Rosenberg, W. M. J. Green, S. Assefa, D. M. Gill, T. Barwicz, M. Yang, S. M. Shank, and Y. A. Vlasov, "A 25 Gbps silicon microring modulator based on an interleaved junction," Opt. Express **20**(24), 26411–26423 (2012).
19. D. M. Gill, W. M. J. Green, S. Assefa, J. C. Rosenberg, T. Barwicz, S. M. Shank, H. Pan, and Y. A. Vlasov, "A figure of merit based transmitter link penalty calculation for CMOS-compatible Plasma-Dispersion Electro-Optic Mach-Zehnder modulators," (2012). http://arxiv.org/abs/1211.2419.
20. X. Tu, T.-Y. Liow, J. Song, M. Yu, and G. Q. Lo, "Fabrication of low loss and high speed silicon optical modulator using doping compensation method," Opt. Express **19**(19), 18029–18035 (2011).
21. A. Liu, L. Liao, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, and M. Paniccia, "Recent development in a high-speed silicon optical modulator based on reverse-biased pn diode in a silicon waveguide," Semicond. Sci. Technol. **23**(6), 064001 (2008).
22. J. Ding, H. Chen, L. Yang, L. Zhang, R. Ji, Y. Tian, W. Zhu, Y. Lu, P. Zhou, and R. Min, "Low-voltage, high-extinction-ratio, Mach-Zehnder silicon optical modulator for CMOS-compatible integration," Opt. Express **20**(3), 3209–3218 (2012).
23. V. Lehmann, "Electrochemistry of Silicon", Wiley-VCH(2002).
24. Z. Huang, N. Geyer, P. Werner, J. de Boor, and U. Gösele, "Metal-assisted chemical etching of silicon: A review," Adv. Mater. **23**(2), 285–308 (2011).

1. Introduction

During the last decade silicon nanophotonics is emerging as a key platform for the miniaturization of various optical devices and systems. The introduction of electro-optic functionalities into complementary metal-oxide-semiconductor (CMOS) technology holds a great promise for monolithic integration of electrical and optical components on the same chip and enables the realization of miniaturized, integrated photonic circuitry. Taking advantage of both the robust nano electronics technology and the mature, well established silicon fabrication process, CMOS manufacturing is expected to provide a reliable solution for developing high yield, large scale and low cost active nanophotonic devices.

One of the critical elements for on-chip photonic applications is the silicon electro-optic (EO) modulator. Due to weak EO effect, optical signal modulation in silicon is often achieved via the free carrier (FC) plasma dispersion effect, where the changes in free-carriers concentration induce variations in both real and imaginary parts of the complex refractive index [1]. Among other potential solutions, such as incorporation of various EO polymers [2] and germanium [3, 4] into the silicon platform, the FC-effect based devices show higher degree of CMOS compatibility and fabrication simplicity. For these reasons, nowadays common construction of silicon EO modulators relies on the incorporation of electrical diode operating under forward (injection) or reverse (depletion) bias conditions into photonic structures such as microring resonators or Mach-Zehnder interferometers (MZI) [5–14], having the role of converting the induced refractive index changes in the silicon waveguide to an optical intensity modulation at the modulator output. Typically, the operation in depletion mode provides higher modulation speed and lower power consumption as compared to injection type devices due to majority carriers drift process at reverse bias and negligible leakage current, respectively [5]. As for the optical design, a MZI configuration offers higher

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bandwidth and robustness at the expense of larger footprint compared to resonant photonic structures [5].

Traditional challenges in optimization of silicon EO modulators are related to the weak nature of the plasma dispersion effect and the inevitable optical losses induced by the free-carrier absorption. The electro-optic modulation efficiency is usually quantified by the π-phase-shift voltage-length product ($V_\pi L$) with the goal of reducing this parameter as much as possible. In the case of depletion-mode PN junction based modulators, the crucial factors for obtaining high modulation efficiency are related to the doping profile of the junction and the degree of the overlap between the space charge regions of the diode and the optical mode [10–14]. Therefore, in the conventional approach of using vertical or horizontal PN junction configurations, the efficiency of EO modulation is highly dependent on the junction position within the waveguide with the goal of aligning the depletion region variations to match the maximum of the optical mode intensity. Misalignment of junction position would typically result in low modulation efficiency. Recently, the concept of periodically interleaved PN junctions arrangement, where the P- and the N-type regions of the diode alternate along the waveguide, was outlined and experimentally demonstrated for the construction of EO silicon modulators [14–18]. The distinctive improvement of this interleaved configuration compared to the lateral designs is associated with better light-carrier overlap and higher junction misalignment tolerance, because upon the application of reverse bias the depletion regions of the interleaved junctions are extended along the optical propagation direction rather than across the waveguide. As a result, the carrier depletion areas would be greatly overlapped with the optical signal inside the waveguide.

In addition to modulation efficiency optimization, not of lesser importance is to minimize the optical losses of the structure [10–14, 19, 20]. Generally speaking, the minimization of optical losses is considered as an essential step toward optoelectronic link budget optimization. In the case of free carrier dispersion mechanism, there is a fundamental tradeoff between the optical loss and the attainable modulation efficiency, since the realization of higher doped PN junction with stronger contribution to the plasma dispersion effect would commonly come at the expense of higher absorption and limited extinction ratio of the modulator. Therefore, the optimization of modulation efficiency and the appropriate doping design should take into account both considerations of reducing the $V_\pi L$ value and at the same time keeping the optical loss of modulator as low as possible [10–14, 19, 20]. As a result, an important figure of merit (FOM) for the design of carrier based EO modulators is the multiplication of $V_\pi L$ parameter and the optical loss per unit length.

In this work we present the study a carrier depletion silicon electro optic modulator with the goal of minimizing the loss-efficiency FOM. We verify the simulation results by fabricating an asymmetric MZI optical configuration where a phase-shifter is realized by a periodically interleaved array of PN junctions operating in reverse bias. By reducing the junction width, together with optimizing the doping levels and doping profile, we obtain high efficiency modulation together with very low free carrier loss, leading to a very low FOM in the order of ~6.7 V-dB. This value is currently the lowest among the carrier depletion type silicon EO modulators operating in MZI configuration.

2. Diode design and optimization

As mentioned above, we adopted the concept of interleaved PN junctions for the construction of the phase-shifter (Fig. 1). It was previously demonstrated [14–18], that interleaved configuration provides higher overlap between the carrier depletion regions and the optical waveguide mode compared to the lateral PN junction approach.

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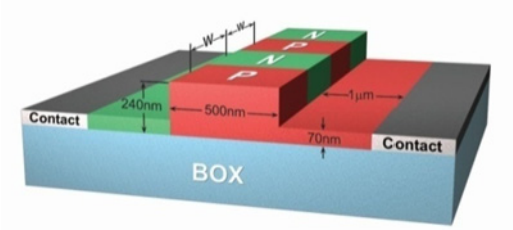

Fig. 1. Schematics of the phase shifter design with periodically (W = 200nm) interleaved PN junctions. A rib like silicon waveguide is positioned on top of 2μm thick buried oxide layer.

As a starting point we calculate the modulation efficiency ($V_\pi L$), free carrier optical loss, and FOM (efficiency-loss) of the phase shifter as a function of the doping concentration for various junction widths (W), as shown in Fig. 2.

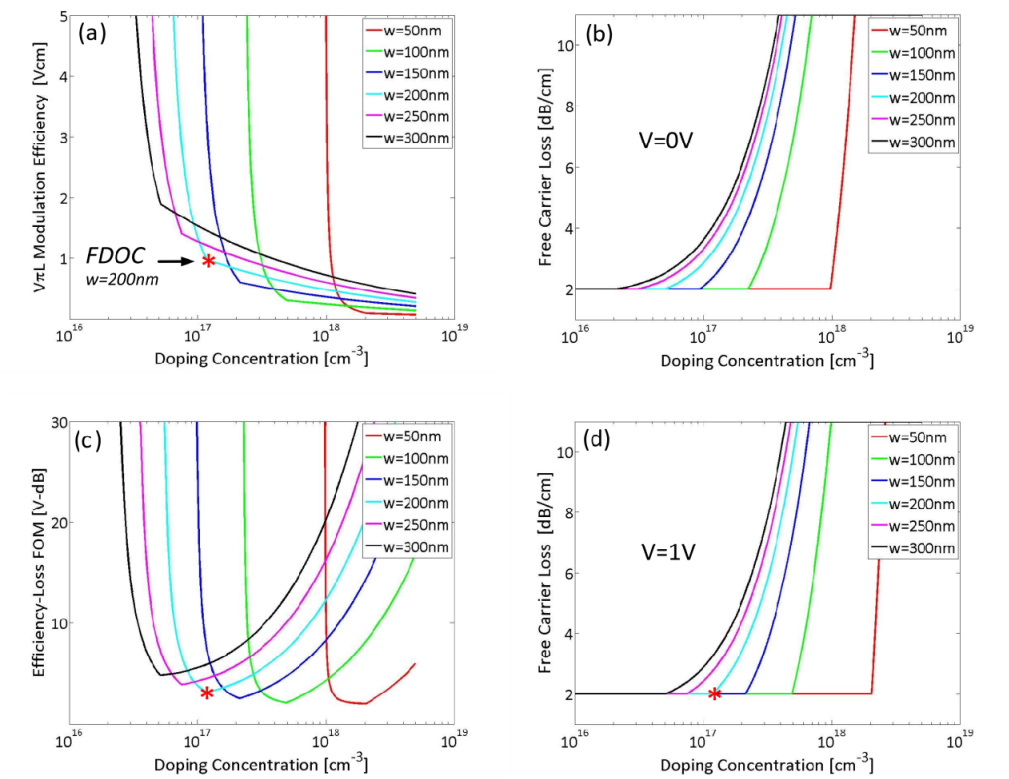

Fig. 2. (a) Modulation efficiency calculated for reverse bias of 1V, (b,d) free carrier loss at 0V and 1V reverse bias respectively, and (c) efficiency-loss FOM of the phase shifter as a function of doping concentration. For FOM calculation we assumed a worst-case scenario of the maximal free-carrier loss corresponded to zero bias and additional 2dB/cm propagation loss due to the waveguide surface roughness. The red star corresponds to full-depletion operation condition (FDOC) for junction width of 200nm. The calculated results assumed mode confinement of 0.84, in agreement with the waveguide cross section dimensions of Fig. 1.

To study the design trends we assumed a step junction with symmetric doping profile. This simplification will be released later on when we discuss actual device fabrication. Throughout the simulations we used the maximum drive voltage of 1V corresponding to the modern CMOS manufacturing technology nodes. Refractive index modulation and free carrier loss of the junction were derived by Soref empirical formula for operation wavelength

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of 1.55μm [1]. The efficiency-loss FOM was calculated taking into account the maximal free-carrier loss at zero bias and the modulation efficiency at reverse bias of 1V. By observing Fig. 2(a), we notice the following trends. First, for low doping levels, the modulation efficiency is negligible, i.e $V_\pi L$ goes to infinity. This is because the junction is already fully depleted at zero bias and thus no modulation occurs. As we increase the doping, the modulation efficiency rapidly improves, because the junction is no longer fully depleted at zero bias and thus its width varies under the application of reverse bias. This rapid improvement continues up to a turning point in the slope of the curve (marked by a red star). This turning point is obtained when the depletion width under the application of the operation reverse bias (1V) exactly matches the physical junction width (W). We define this turning point as the full-depletion operation condition (FDOC). Beyond this point, the modulation efficiency still improves with the increase in doping level, but at a much lower rate. Clearly, the FDOC point depends on the W - reducing the junction width allows achieving the FDOC point at a higher doping level, with the benefit of reducing the $V_\pi L$. Naively, one would seek to increase the doping as much as possible, in order to improve the modulation efficiency. However, further increase of the doping level beyond the FDOC leads to a significant loss due to free carrier absorption (Fig. 2(d)). This loss penalty degrades the device performances. Therefore, the optimization of the doping concentration should be calculated based on the efficiency-loss FOM [11,14,19,20]. In Fig. 2(c) we plot this FOM against the doping concentration for several values of junction widths. Observing Fig. 2(c), we notice the existence of an optimal doping concentration for each junction width. The optimum occurs at the FDOC point, where the maximal depletion region width at reverse bias match of the junction dimensions (W) and therefore allowing a significant portion of the waveguide volume to contribute to refractive index modulation. Considering fabrication tolerances, it seems to be more practical to choose doping levels slightly above the FDOC point. This is because a minor reduction in doping concentration below the FDOC point results in severe degradation in modulation efficiency as evident by the abrupt increase in $V_\pi L$, implying the need for a much longer phase-shifter. On the other hand, slight increase in doping level above the FDOC point has only a little effect on the FOM side by side with lower $V_\pi L$. Additionally, from Fig. 2(c) we notice that the optimal FOM can be improved by choosing smaller values of W. This is because reducing the junction width allows the use of higher doping concentrations for operation near the FDOC point, and as a result provides higher modulation efficiency without increasing the optical absorption at fully depletion operation condition.

Together with the optimization of modulation efficiency and FOM, another important performance metric of silicon electro-optic modulator is the operation speed of the device. Nowadays, the state of the art commercial modulators are expected to operate at tens of Gb s^{-1} regime and to support the ever-increasing bandwidth demand of modern communication networks. The high-speed performance of the MZI modulator depends on careful design and optimization of traveling-wave coplanar waveguide (CPW) electrodes, optical waveguide properties, doping profile (level) and electrical parameters of PN junction integrated into the phase-shifter [12,14,17, 21,22]. A common RF design approach in MZI modulators is based on modeling the phase-shifter as a capacitive-load transmission line (TL), where typical optimizations include a) obtaining similar velocity for microwave and optical signals, b) minimizing transmission-loss as much as possible and c) matching the characteristic impedance of TL to driver impedance and to termination resistor. For depletion-type modulators the capacitive-load is represented by junction capacitance and serial resistance of the diode, which values are highly dependent on doping concentration and junction dimensions [12,14,17, 21,22].

In the case of interleaved phase shifter design, the optimization of modulation efficiency and FOM is directly related to reducing the junction width with consequent employment of higher doping level in order to perform near the fully depleted operation condition (as discussed previously, see Fig. 2). As a result, one could expect a trade-off between obtaining

#192248 - $15.00 USD Received 14 Jun 2013; revised 27 Jul 2013; accepted 29 Jul 2013; published 12 Aug 2013

higher modulation efficiency and increase of junction capacitance, which in turn implies higher delay of transmission line and lower operation speed. Figure 3(a) shows the intrinsic 3dB bandwidth of capacitive-load of a single diode segment plotted for different junction width as a function of doping concentration. The intrinsic bandwidth was calculated according to at $BW_{3dB} = 1/2\pi R_s C_D$ reverse bias of 1V, where R_S and C_D are the diode capacitance and serial resistance respectively. Throughout the calculations we assumed a step junction with symmetric doping profile.

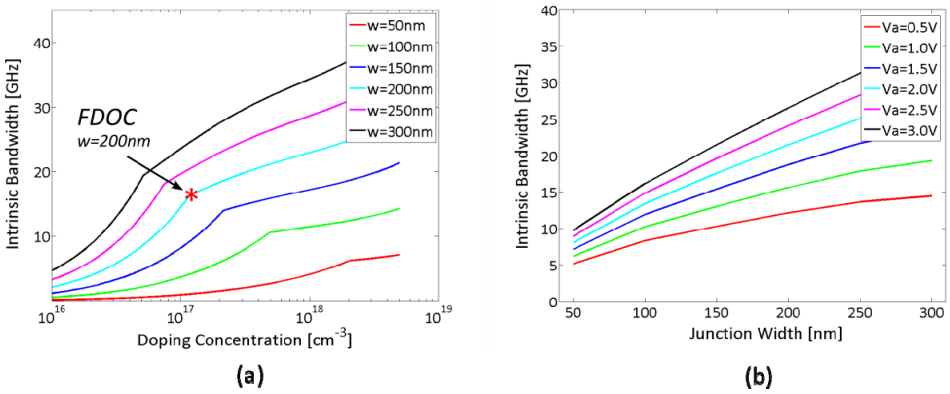

Fig. 3. (a) Intrinsic 3dB bandwidth of a single diode segment at reverse bias of 1V for different junction widths as a function of doping concentration. b) Intrinsic 3dB bandwidth of a single diode segment at fully-depleted operation condition for different reverse biases as a function of the junction width. Throughout the calculations a step junction with a symmetric doping profile is assumed.

According to Fig. 3(a), for doping concentration below the FDOC point the intrinsic 3dB bandwidth of increases with the doping concentration primarily due the reduction in serial resistance, whereas the capacitance is kept constant because the junction remains fully depleted for reverse bias of 1V. A turning point in the slope of the curve can be clearly observed at FDOC point. For higher doping levels beyond the FDOC point, the bandwidth is still improved, however at a considerably slower rate. This corresponds to the fact that together with the continuous reduction in serial resistance, the capacitance is increased, because the junction is already not fully depleted and the depletion regions shrink with the increase in doping concentration. Moreover, by observing Fig. 3 one could notice the reduction of bandwidth as a result of using smaller junctions, demonstrating the tradeoff between modulation efficiency, FOM and operation speed. Therefore, we believe that it would be not beneficial (in terms of bandwidth) to reduce the junction width of the phase shifter much below 100nm.

Based on these observations, we turn into the design of our modulator with the goal of achieving low value of efficiency-loss FOM. First, taking into account the limitation of our lithography process and the need for potentially high bandwidth we set the width of doped regions to be 200nm. Additionally, we considered the maximal operation voltage of 3V as a compromise between the desire for low voltage operation and the need for short phase-shifter length. Figure 4 presents the calculated $V_\pi L$ and FOM of a phase shifter with embedded 200nm wide interleaved junctions. We assumed a step junction with a symmetric doping profile, and the results are presented for various reverse biases as a function of doping concentration.

As can be seen, the modulation efficiency slightly reduces with the increase in operation voltage, as evident by the increase in $V_\pi L$. This result, which was also reported in previous works [14], is due to the fact that the depletion region width varies with the operation voltage in a sub linear fashion. Additionally, we also note that the FOM increases with the operation

#192248 - $15.00 USD Received 14 Jun 2013; revised 27 Jul 2013; accepted 29 Jul 2013; published 12 Aug 2013

voltage. This is not only because of the increase in $V_\pi L$ but primarily because of considering the worst-case scenario in which the loss was taken at zero bias for any application voltage. In practice, the degradation of the FOM with the increase in operation voltage may become less prominent if one uses loss values calculated at half of the maximal voltage as proposed by [19]. Taking into account the calculated confinement factor of optical mode in silicon waveguide core to be ~0.84, in agreement with the waveguide cross section dimensions of Fig. 1, we estimated (Fig. 4) the doping concentration at FDOC point under reverse bias of 3V to be $\sim 2.4\cdot 10^{17}\,\mathrm{cm}^{-3}$. As mentioned above, we chose to work with doping levels slightly beyond the simulated FDOC point and designed the ion implantation process to obtain dopants concentration in the order of $4\cdot 10^{17}\,\mathrm{cm}^{-3}$.

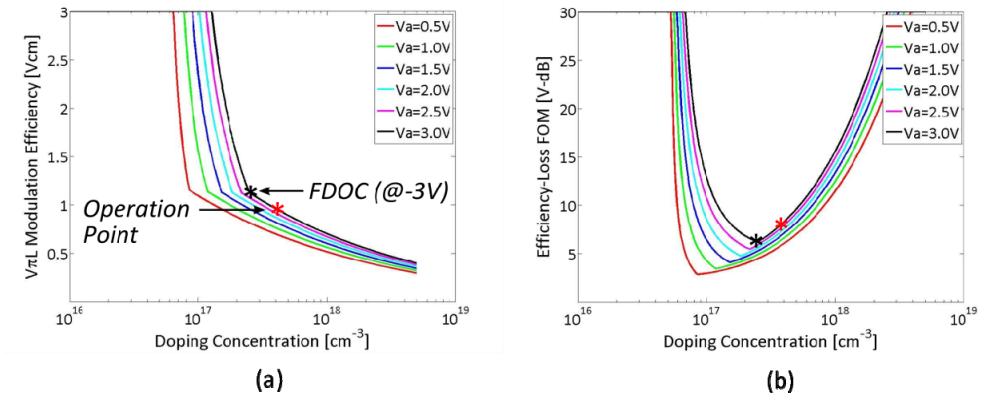

Fig. 4. (a) Modulation efficiency and (b) efficiency-loss FOM of the phase shifter with embedded 200nm wide interleaved junctions as a function of doping concentration calculated for different reverse biases. For the FOM calculation we assumed a worst-case scenario of the maximal free-carrier loss corresponded to zero bias and additional 2dB/cm propagation loss due to the waveguide surface roughness. The calculated results assumed mode confinement of 0.84, in agreement with the waveguide cross section dimensions of Fig. 1.

While the above discussion was based on the assumption of symmetric step junction, the real doping profile deviates from this ideal scenario. In order to precisely estimate the doping profile of our designed device, we used a commercial software package SILVACO to simulate different aspects of the fabrication process including the ion-implantation, annealing and dopants diffusion (ATHENA module),together with static electrical simulations of a junction segment under application of different reverse biases (ATLAS module). To simulate the ion-implantation both for Boron and Phosphorus dopants we assumed a 20nm thick screening oxide layer, similar to our actual fabrication parameters, and used the dual Pearson model to take the ion-channeling effect into account.The subsequent annealing and dopants drive processes were simulated based on fully-coupled pair diffusion model which includes two-way interactions between the diffusion of dopants and diffusion of the points defects. After obtaining a doping profile at thermodynamic equilibrium, we moved towards the electrical analysis, where the program (ATLAS) numerically solves the coupled Poisson's equation and the charge continuity equation for electrons and holes to simulate the free carriers distribution inside the junction for different bias conditions. The following semiconductor physics models, namely the Shockley-Read-Hall and Auger recombination models with doping-dependent lifetime, the doping-dependent and field-dependent mobility model and the silicon bandgap narrowing model were included in the electrical simulations. Figure 5(a) shows the calculated profiles of electrons and holes in a single diode segment under different bias conditions, as taken from the numerical simulations of an interleaved phase-shifter with junction period of W = 200nm.

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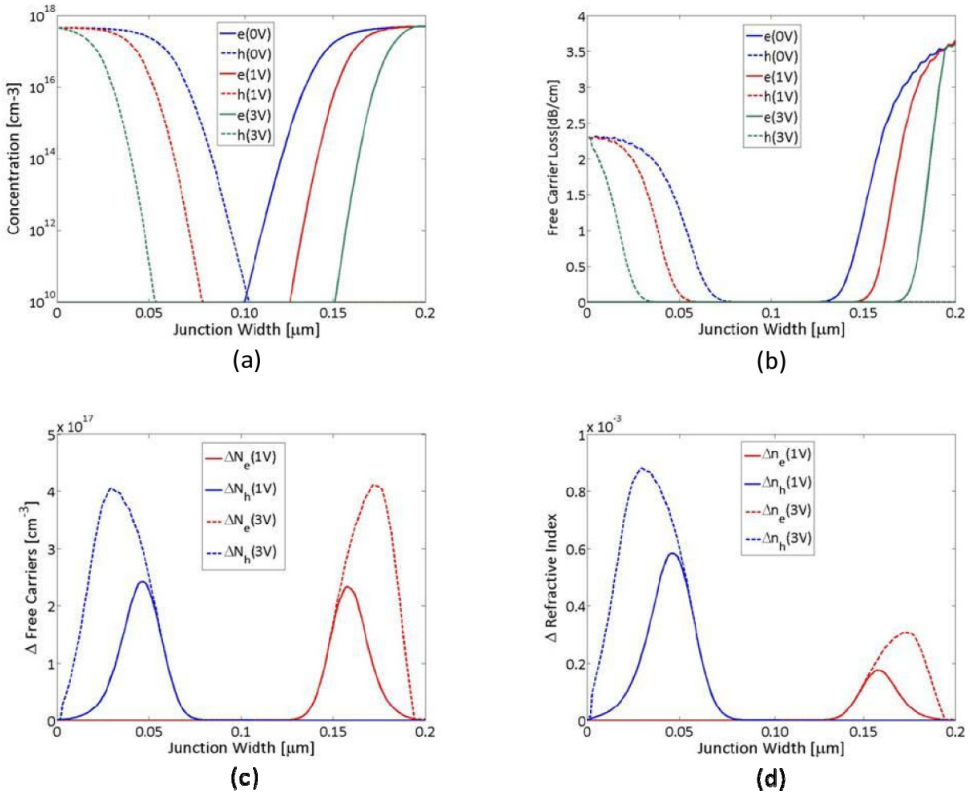

Fig. 5. a) Free electrons and holes concentrations inside a single PN junction along the optical propagation direction for different reverse biases of 0V, 1V and 3V. b) Free carrier absorption loss profile along a single PN junction for different reverse biases of 0V, 1V and 3V. c) Free carriers variations profile along a single junction as a result of reverse bias application. d) Refractive index modulation profile along a single PN junction corresponding to the free carriers variations.

By using Soref's empirical formula [1] and the data presented in Fig. 5(c), we calculated the free carrier loss profiles and the refractive index variation along the waveguide direction for a single diode segment (Fig. 5(b) and 5(d)). Based on these results we estimated the effective refractive index modulation in the silicon waveguide by integrating the refractive index changes over the junction width and normalized this value to the diode width (e.g. 200nm). We found the net refractive index variation contributed by a single PN junction with doping concentrations of $\sim 4\cdot 10^{17}\,\mathrm{cm}^{-3}$ operating under reverse bias of 3V to be in the order of $2.2\cdot 10^{-4}$. In a similar manner we found the amount of free carriers optical loss in the waveguide (Fig. 5(b)), and obtained attenuation constants of 0.54 dB/mm and 0.12 dB/mm for zero and reverse bias of 3V respectively. For lower reverse bias operation of 1V, which is now desired by many electronic systems [18, 19], the simulations predict net refractive index changes of $\sim 1\cdot 10^{-4}$ with free carriers optical loss of 0.39 dB/mm.

3. Device fabrication

Our device was fabricated using SOI substrate with 250nm thick silicon device layer on top of a 2 μm thick buried oxide. First, we applied a p-type base doping level in the silicon device layer by a single peak boron implantation ($D = 1.3\cdot 10^{13}\,\mathrm{cm}^{-2}$, $E = 45\,\mathrm{kV}$) through a thin (~20nm) thermally grown silicon oxide layer for preventing channeling of light boron dopants. Following the implantation, the sample was annealed for 45min at 1000° C. Next, the

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optical structure consisting of an asymmetric MZI was defined by e-beam lithography (Raith 150 eLine) followed by 170nm deep reactive ion etching of silicon (Oxford Plasmalab 100) to transfer the pattern into device layer. We used both Y-splitters and multi-mode interference (MMI) devices to split and combine the optical beam and observed decent operation in both configurations. The constructed 500nm wide and 240nm high silicon waveguide with a rib thickness of 70nm supports a single TE (in-plane) polarized optical mode. The periodically interleaved PN junctions were created in both arms of the MZI in order to balance the optical loss. For this reason, phosphorus (Ph) dopants were implanted into the p-type silicon waveguide using a 200nm thick aluminum mask of the interleaved configuration, which was realized by e-beam lithography and lift-off processes. We performed two peaks phosphorus implantation ($D_1 = 0.8 \cdot 10^{13}\,\mathrm{cm}^{-2}$, $E_1 = 60\mathrm{kV}$, $D_2 = 3.2 \cdot 10^{13}\,\mathrm{cm}^{-2}$, $E_2 = 110\,\mathrm{kV}$) in order to form homogeneous Ph concentration all over the n-type areas and to vertically align a metallurgical junction of the diode to be perpendicular to the light propagation direction in the waveguide (Fig. 6(a)). The actual B and Ph doping concentrations were derived from 4-probe resistivity measurements and were found to be $\sim 4.3 \cdot 10^{17}\,\mathrm{cm}^{-3}$ and $\sim 4.1 \cdot 10^{17}\,\mathrm{cm}^{-3}$ respectively.

To test the formation of interleaved doping pattern and the alignment of the junction array along the waveguide we performed a selective shallow etching of Boron (p-type) areas of test sample using buffered HF solution (BHF). Silicon can be dissolved in HF solution both by electrochemical [23] and by metal assisted etching [24]. Both techniques rely on the presence of holes (h^+) at the silicon interface, where either external bias or metal catalysts are typically employed for achieving substantial etching rate. Here, in order to reveal the interleaved junction profile of the phase-shifter we were interested in slow process to perform only a shallow (~tens of nanometers) etching of silicon. Therefore, we used neither voltage bias nor metallic catalysts during the etching and mostly relied on the presence of free holes in the semiconductor itself. Consequently, the etching rate was dramatically reduced, so that we experimentally observed ~80nm thick, selective etching of p-type silicon area after dipping the sample in BHF for two hours (see Fig. 6(b)).

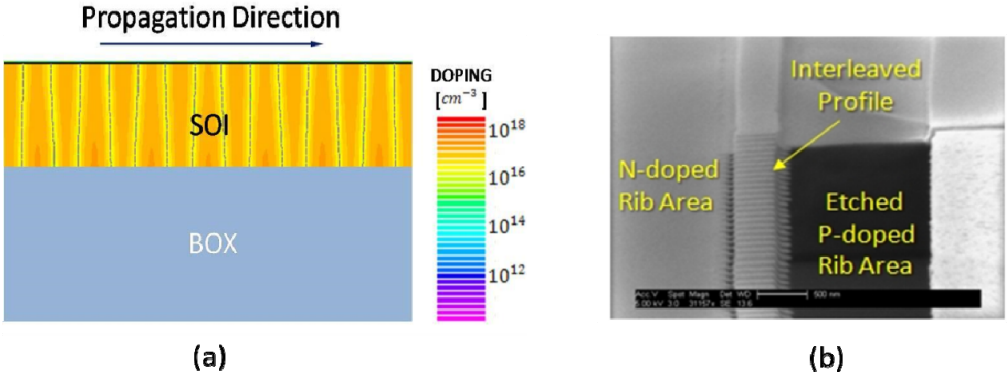

Fig. 6. a) Process simulation results of interleaved doping profile at the center width of the waveguide along the light propagation direction. The obtained metallurgical junctions (black dashed lines) are vertical and nearly perpendicular to the light propagation direction. b) Scanning electron micrograph of the test sample after selective shallow etching of the p-type (boron doped) regions of the phase shifter. The interleaved doping pattern is easily observed along the phase shifter. The obtained junction extensions into the rib areas are in the order of 70nm.

According to result presented in Fig. 6(b), the formation of the interleaved doping pattern along the phase shifter could be easily observed, including ~70 nm extension of the junction into the rib areas. To the best of our knowledge this is the first time that such a selective etching method is applied for the visualization of the junction geometry. Finally, ohmic

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contacts were formed by deposition and alloying aluminum electrodes (420° C) on top of the highly doped silicon areas, which were located 1μm away from the waveguide. An optical microscope image of a typical fabricated device is shown in Fig. 7:

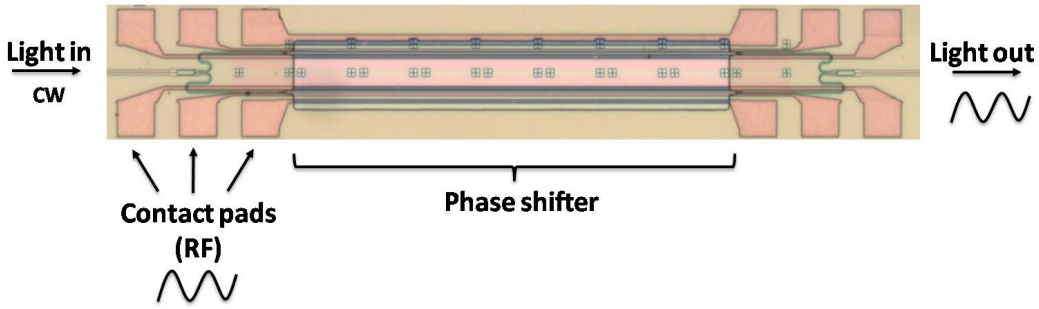

Fig. 7. Optical microscope top view of the fabricated device. The MZI waveguides and the contact pads can be clearly observed.

4. Device characterization

The modulation efficiency and the FOM values of the fabricated device were estimated from the optical transmission spectra measurements taken under several reverse biases. The transmission spectrum at each operation voltage was measured by butt coupling a TE polarized light from a tunable laser source (Agilent 81680A) into the input facet of the waveguide using a polarization maintaining lensed fiber with mode size of ~2.5μm. At the output facet, the optical signal was collected with a similar fiber and detected by an external InGaAs photodetector (Agilent 81634a). Figure 8(a) shows the measured transmission spectra of an unbalanced (160μm difference) MZI-modulator with a 1.4mm long phase shifter at different reverse biases. The reverse bias was applied to a single arm of the MZI while the other arm was fixed at zero bias. Results are normalized to a reference undoped waveguide. The insertion loss is estimated to be ~4 dB which is the results of slightly less than 1.5dB loss in each of the two Y splitters (estimated from independent near field scanning optical microscope measurements) and free carrier absorption loss (~1 dB, shown later in Fig. 9).

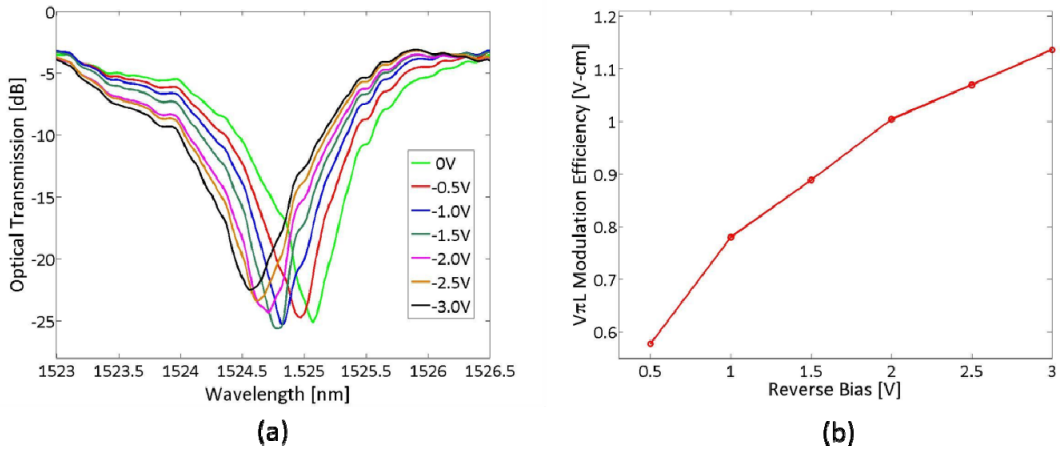

Fig. 8. a) Transmission spectrum measurements of a MZI-modulator with 1.4mm long phase shifter operating under different values of reverse bias. b) Experimentally measured $V_\pi L$ values as a function of applied reverse bias.

The relative phase shift $\Delta\varphi$ as a function of reverse bias was extracted from the transmission spectra by using the relation $\Delta\varphi = 2\pi \cdot \Delta\lambda / \mathrm{FSR}$, where $\Delta\lambda$ is the relative

#192248 - $15.00 USD Received 14 Jun 2013; revised 27 Jul 2013; accepted 29 Jul 2013; published 12 Aug 2013

wavelength shift due to the application of reverse bias, and FSR is the free spectral range of unbalanced MZI structure that was found to be 3.36nm. Based on the experimental data extracted from Fig. 8(a), we calculated the refractive index changes in the phase shifter to be $\sim 0.95\cdot 10^{-4}$ and $2\cdot 10^{-4}$ for reverse biases of 1V and 3V respectively. These results come in close agreement with the process simulation predictions of $1.07\cdot 10^{-4}$ and $2.28\cdot 10^{-4}$, which were calculated based on the measured doping levels of $\sim 4.3\cdot 10^{17}\,\mathrm{cm}^{-3}$ and $\sim 4.1\cdot 10^{17}\,\mathrm{cm}^{-3}$ for B and Ph respectively (as extracted from four probe measurement). Next, the modulation efficiency $V_\pi L$ was deduced from $\Delta\varphi$ by using the following expression $V_\pi L = \pi \cdot V_R L_{ph} / \Delta\varphi$ where V_R is the applied reverse voltage and L_{ph} is the phase shifter length of 1.4mm. According to Fig. 8(b), the obtained modulation efficiency for reverse voltages of 1V and 3V are 0.78Vcm and 1.12Vcm respectively, very similar to the simulated values of 0.7Vcm and 0.98Vcm.

To experimentally test the efficiency-loss FOM of our device we characterized the free carrier loss of the fabricated phase shifter, by performing transmission measurements of the device for different reverse voltages, when the same bias was applied to both arms of the MZI. Under such a configuration, we anticipate similar phase accumulation in both arms of the interferometer with negligible wavelength shift, while at the same time the transmission amplitude is expected to vary according to degree of carrier depletion inside the waveguide. Figure 9 shows the experimental results of the free carrier loss measurements.

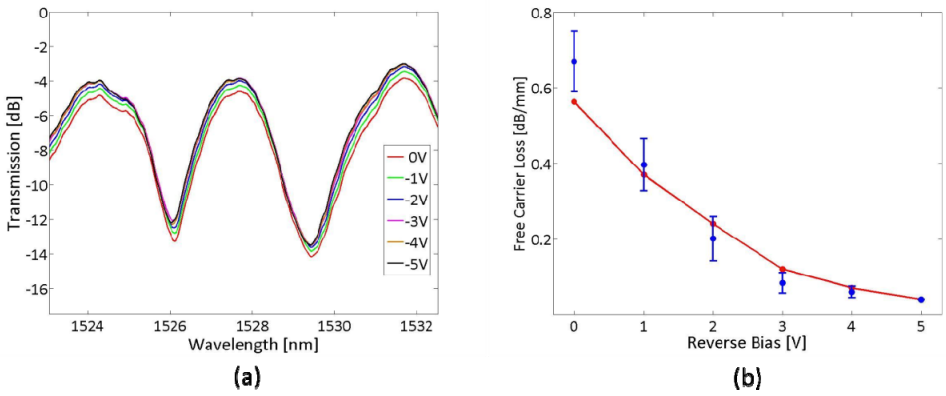

Fig. 9. a) Transmission spectrum measurements of a 1.4mm long phase shifter at different operation voltages, when the reverse bias is applied on both arms of MZI. b) Free carrier loss derived from Fig. 9(a) by measuring the differences in peak transmission as a function of the reverse bias. Results were obtained by averaging over five consecutive transmission peaks. The free carrier loss at reverse bias of 5V is estimated from the process simulations using the measured doping levels. For comparison, we also plot the simulated free carrier loss curve.

According to Fig. 9(a), the measured spectra show negligible wavelength shift when the operation voltage applied to both arms of the modulator, as expected. Additionally, one can observe an increase in transmission for applied reverse bias up to ~3V, and its saturation for higher reverse bias. We attribute the saturation to nearly fully depleted operation, where the free carrier absorption in the phase shifter becomes insignificant compared to the other loss mechanisms and therefore the transmission is independent on applied voltage. Figure 9(b) shows the measured free carrier loss for different reverse voltages as extracted from the transmission peaks of Fig. 9(a), alongside with the calculated curve. Small residual loss can still be observed at high reverse bias values. In the junction there are always free carriers at the region close to the far edge of the depletion layer. This is a direct result of the majority carrier concentration which gradually decreases following the Fermi-Dirac statistics. However, their effect is negligible. Very rapidly the concentration reduces below ~10^{17} cm^{-3}

#192248 - $15.00 USD Received 14 Jun 2013; revised 27 Jul 2013; accepted 29 Jul 2013; published 12 Aug 2013

providing negligible free carrier loss. Yet, this concentration is high enough to enable effective charging of the full depletion layer. To verify the marginal effect of the carriers we measured the loss at even high voltage and could not observe any change in transmission. Moreover, we could not observe significant transmission difference between undoped MZI and our device under large reverse bias. Clearly, the slight difference in loss (if any) is screened by variations in coupling condition from the external fibers to the device. Overall, the measured data agree well with the simulated curve. The small differences can be explained by the fact that the simulated curve is extracted from a 1-D model.

Based on the measured $V_{\pi}L$of 0.78 V-cm, and the free carrier loss at zero bias of 6.6 dB/cm, we can now calculate the efficiency-loss FOM of our device to be in the order of 6.7 V-dB. This is the lowest FOM value reported in the literature so far for carrier depletion silicon MZI modulator.

5. Conclusions

In summary, we demonstrated the design, optimization and experimental characterization of a silicon carrier-depletion MZI EO modulator with the lowest efficiency-loss FOM of about 6.7V-dB. This result was obtained by the use of the periodically interleaved phase shifter configuration with small junction width of 200 nm. The doping levels were optimized in order to operate in nearly fully depleted mode. By doing so, free carrier loss can be significantly reduced.

Additionally, we provide guidelines for the optimization of the device parameters and show that optimum is obtained for operation near the FDOC point. It is also shown that the FOM can be improved by further reduction of the junction width, followed by increasing the doping levels. This will also have a beneficial effect on the modulation efficiency, which in turn will allow the implementation of a shorter phase shifter and/or the operation under even smaller bias. Based on our demonstration results, and given the fact that the interleaved configuration was shown to operate in tens of GHz regime [14–18], we believe that the design considerations and the experimental results presented in this work can benefit the construction of silicon EO modulators with high modulation efficiency and low loss. While the current device was not optimized for high speed operation (e.g. high contact resistance), our future work will also address the bandwidth of the device.

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